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PCB STACK UP  
6L

LAYER 1 : TOP
LAYER 2 : VCC
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : GND
LAYER 6 : BOT

BOM select

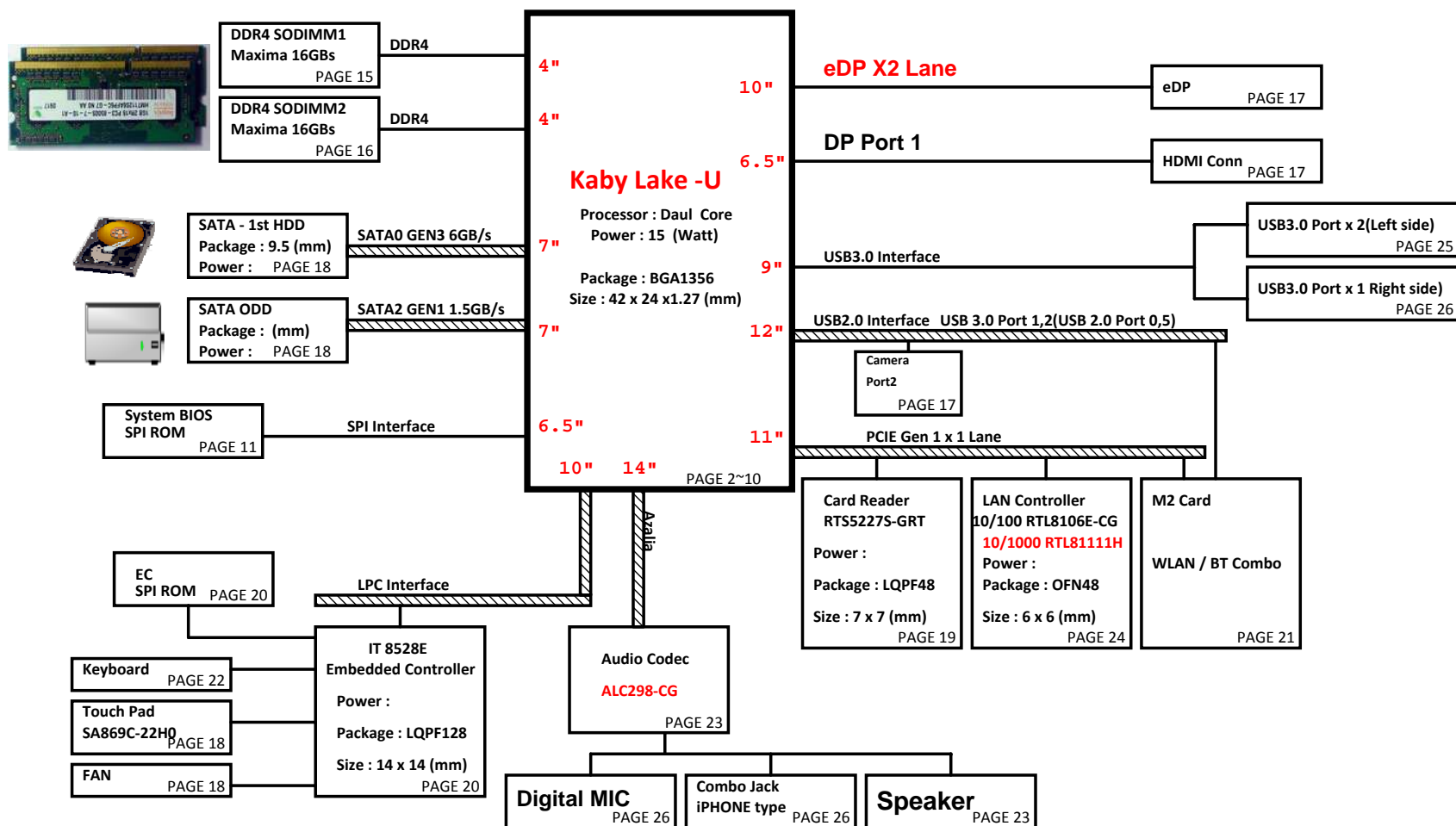
XDP@: XDP
* : No mount

F/W List

	Location	Update method
BIOS/ME	U3	Flash tool in Windows
EC	KU4	Flash tool in Windows

# FFK 15.6" Ultra/Slim Intel Kaby Lake U Platform Block Diagram

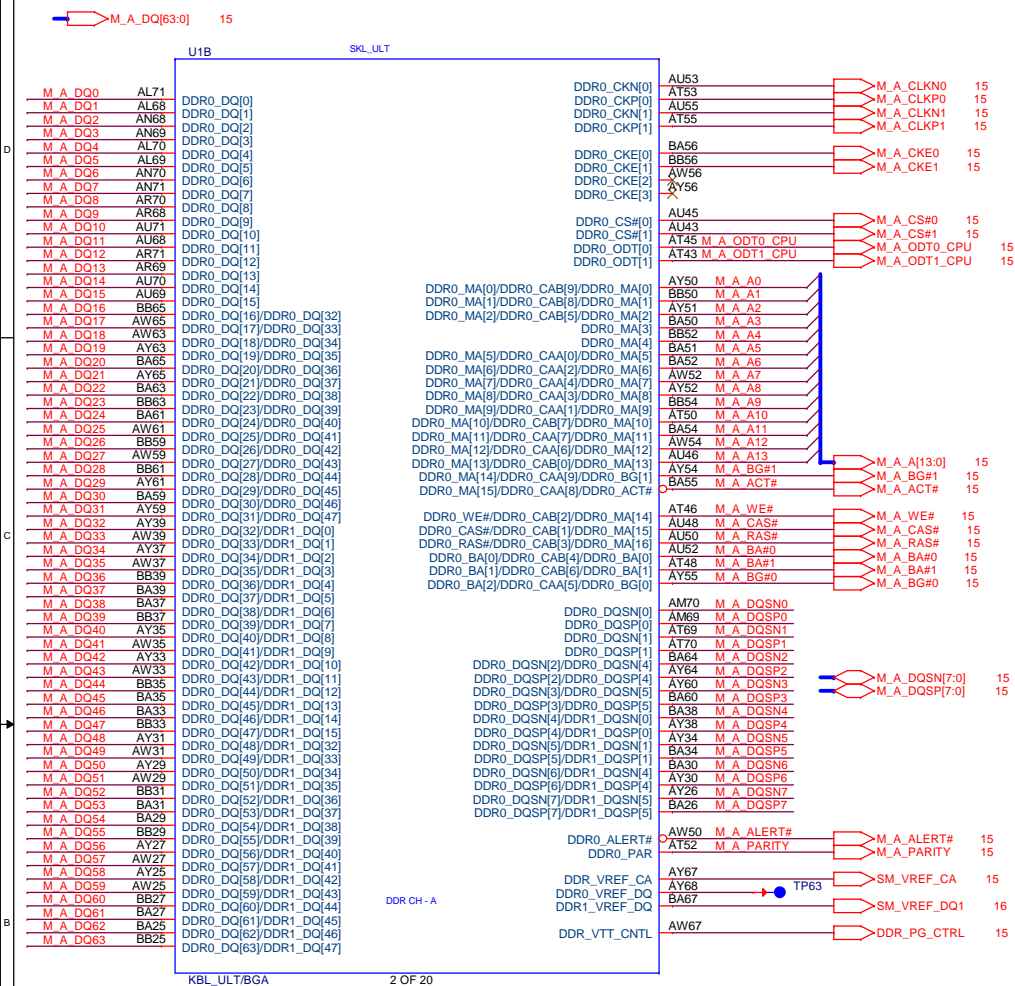
laptoprepairsecrets@gmail.com



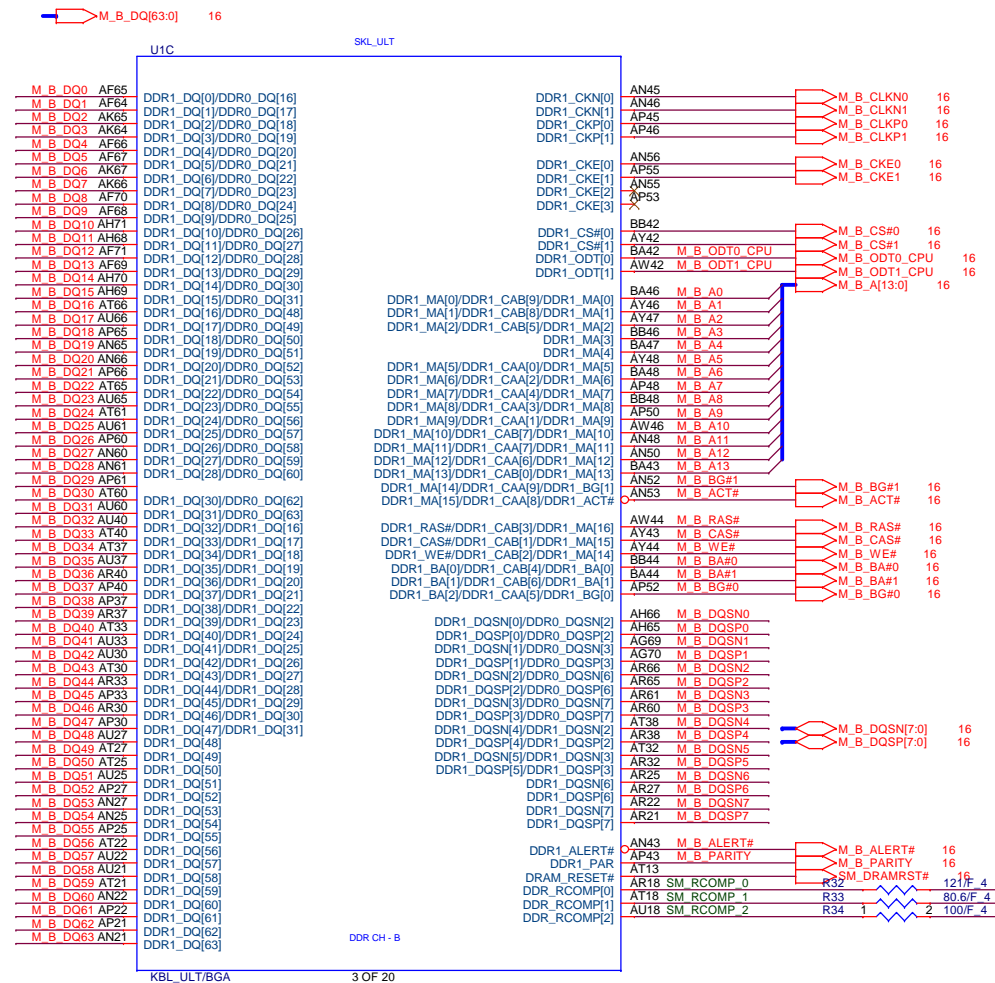
REV		CHANGE LIST						
ES2	1	AR26, R5164, R5165, R5166, R5167 change to short pad						
	2	CN27 2IN1 CARD change to footprint sdcard-psdbtm-09glbs1nn4hb-smt for correct						
	3	Change EMU_LID GPA5 to GPH1 (Open Drain) for BLON timing.						
	4	Stuff C597 0.01uf for VCCST_PWRGD understood issue.						
	5	Add KR83, KU6 & KC36, KC37 circuit location for tPLT18 timing issue with reserve						
	6	Stuff PR327 & PQ61, MAIND change to RUN_ON for tPLT18 timing issue.						
	7	change PR34 from 137k to 124k ohm to correct IMON						
	8	change PR11 from 2.26k to 1.96k to correct LL						
	9	change location PR1,PR2,PR36,PR37,PR53,PR55,PR352 to short pad from 0 ohm 0402 resistor for ES2 stage.						
	10	Del location PG1, PG18, PG14, PG15, PG16, PG17, PG2, PG8, PG13, PG3, PG10, PG9 and PG12, ER13 short PAD for FFK ES2 Verify schematic.						
	11	PC126 change to 220pf from 2200pf & PC121 change to 680pf from 560pf for audio sequence issue.						
	12	PC35 from 680pF to 1000pF to correct DVID reponse						
	13							
14								
15								
16								
17								
18								
PP	1	Change PR180 0ohm to 100kohm & stuff PC142 0.01uF RC delay timing for meet +1.2V_SUS & +2.5V_SUS sequence timing						
	2	change PR48 from 4.32k to 6.8k ohm to correct DCR error at high temp .						
	3	change PR49 from 316 to 365 ohm to set Min 44A OCP						
	4	change PR30 from 110k to 118k ohm to correct IMON.						
	5	change PR10 from 4.32k to 6.8k ohm to correct DCR error at high temp .						
	6	change PR11 from 1.96k to 2.1k ohm to correct LL.						
	7	change PR5 from 316 ohm to 340 ohm to correct LL and IMON.						
	8	change PR42 from 1.65k to 1.78k to correct LL						
	9							
	10							
	11							
	12							
	13							
	14							
	15							
	16							
	17							
	18							
	19							
MRT	1							
	2							
	3							
DOC NO.		PROJECT MODEL :	FFK	APPROVED BY:		DATE:	2016/10/18	
		PART NUMBER:		DRAWING BY:		REVISION:	3A	

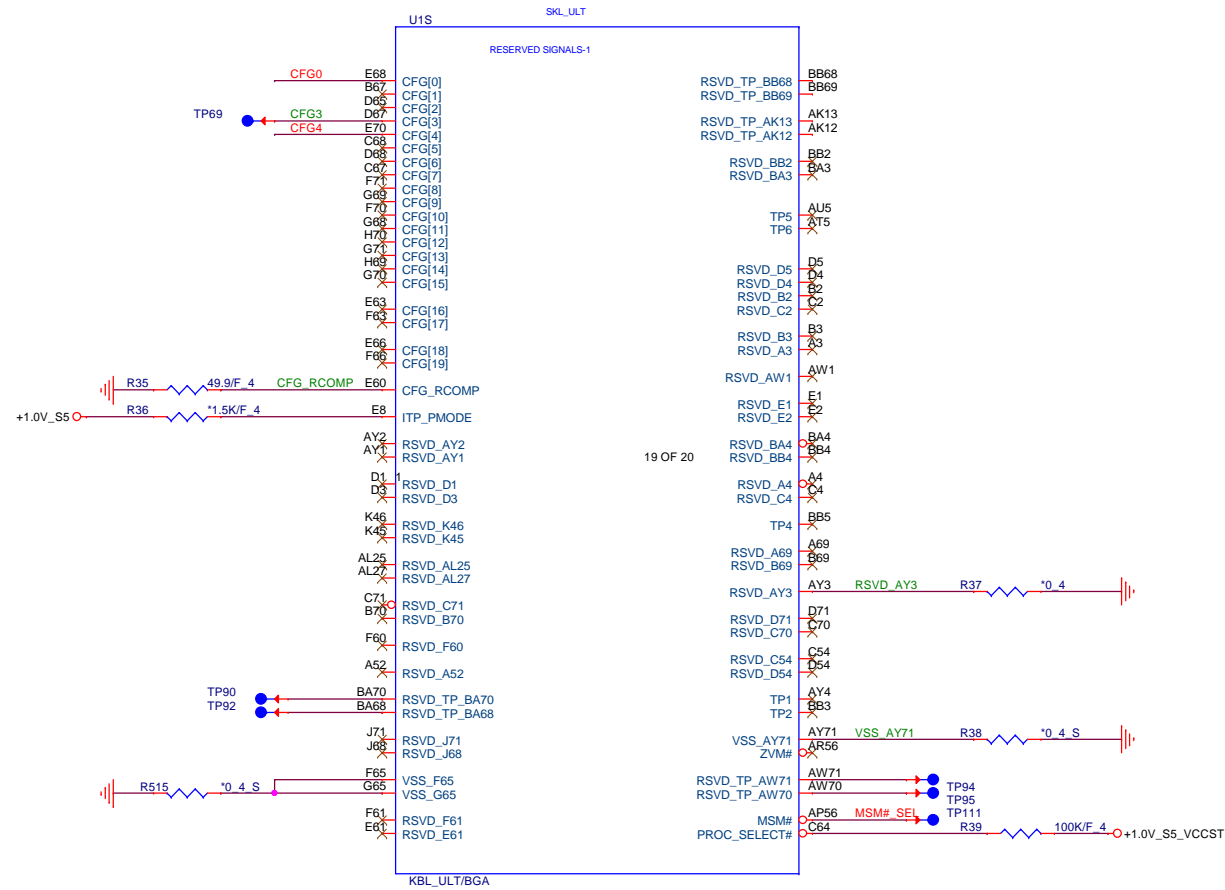


KabyLake ULT (DDR4)



## KabyLake ULT(DDR4)

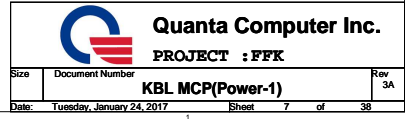


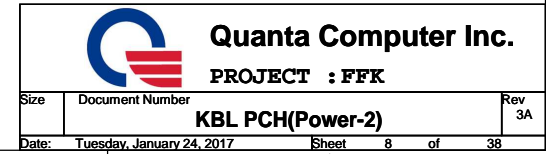


Processor Strapping

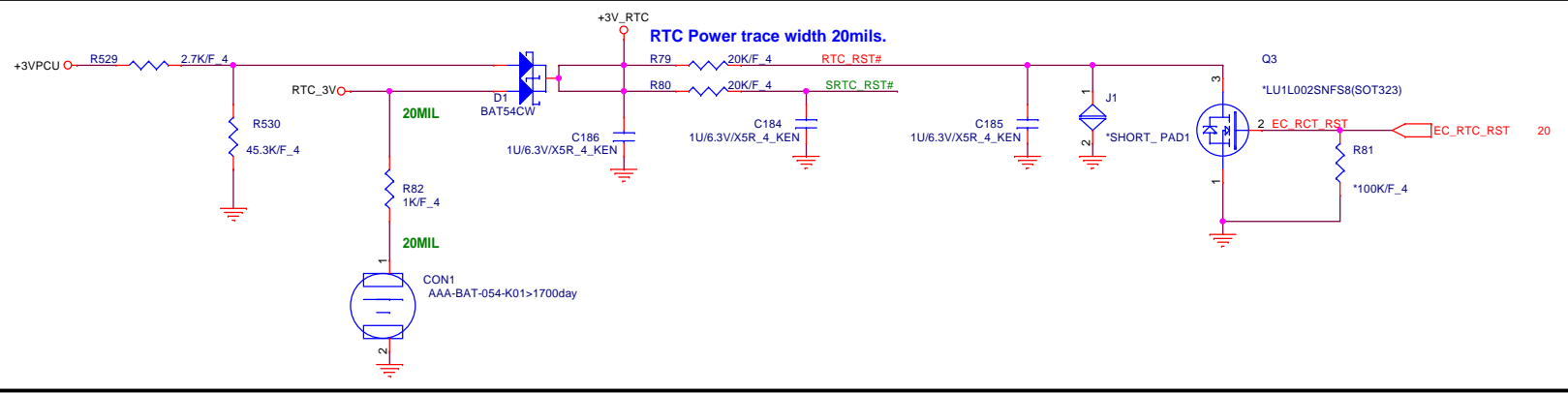
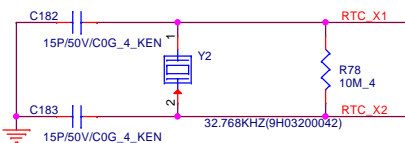
	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	
CFG4 eDP enable:	DISABLED	ENABLED	


## +VCC\_GFX : 22 15W IccMax :31A

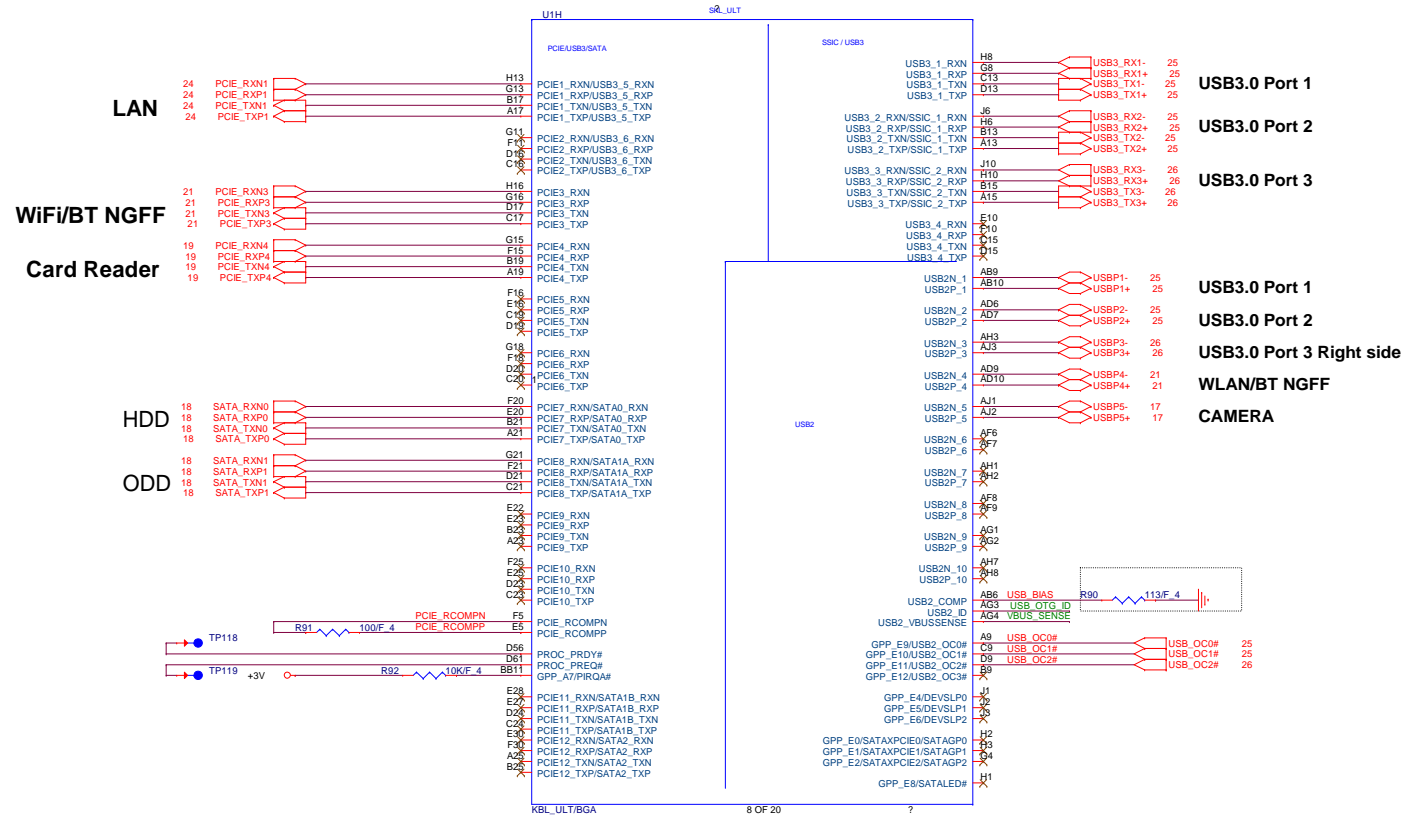






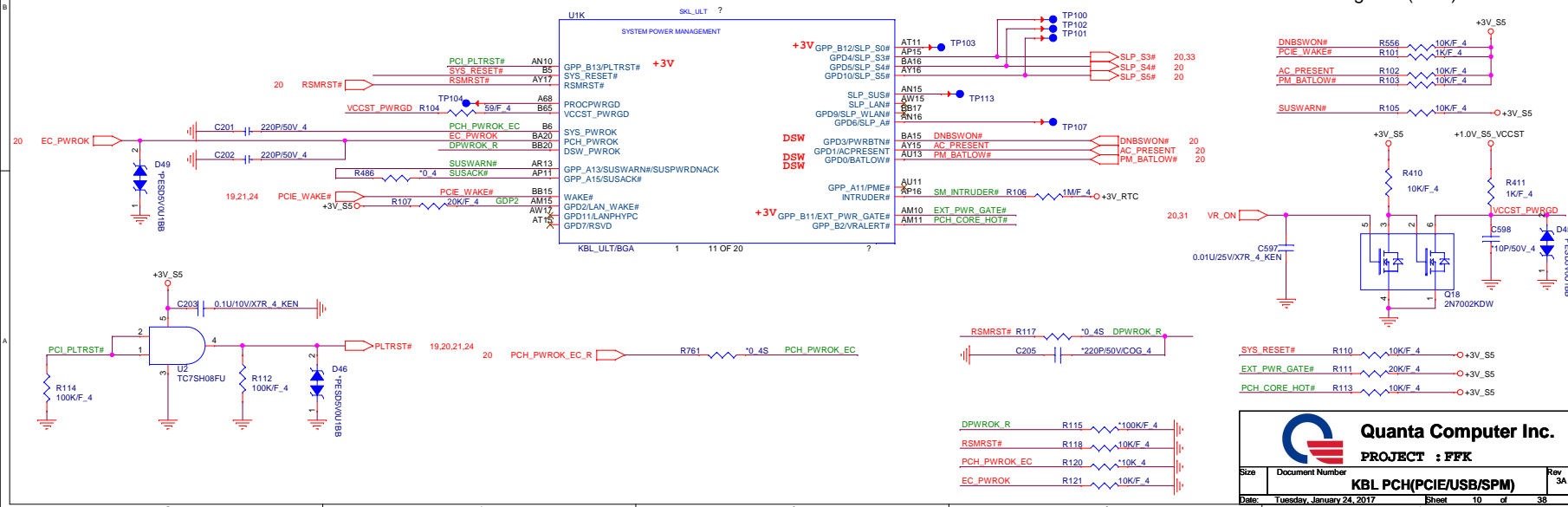


Pin Name	Strap description	Sampled	Configuration	note
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	



## KabyLake ULT (SYSTEM POWER MANAGEMENT)

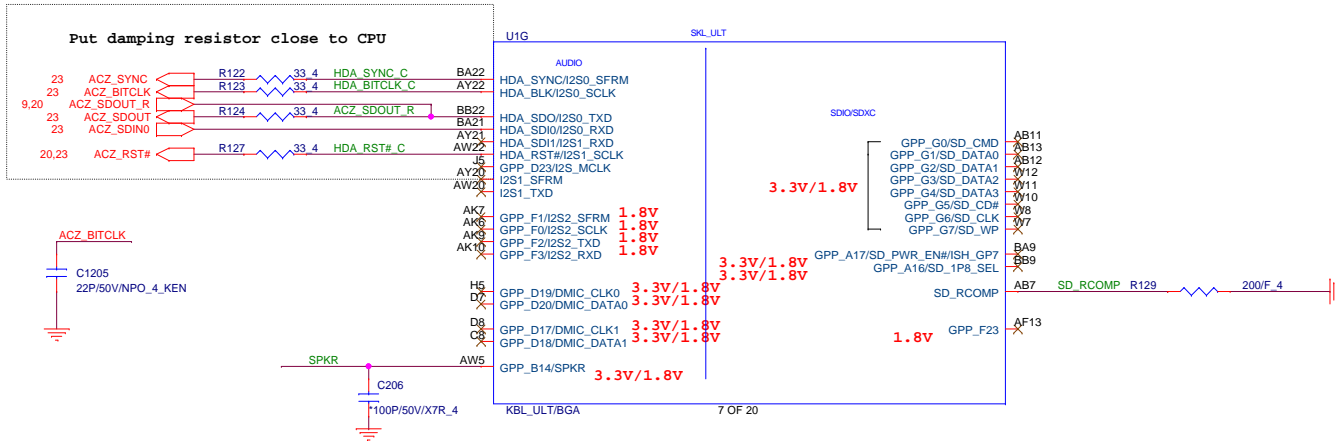
## PCH Pull-high/low(CLG)



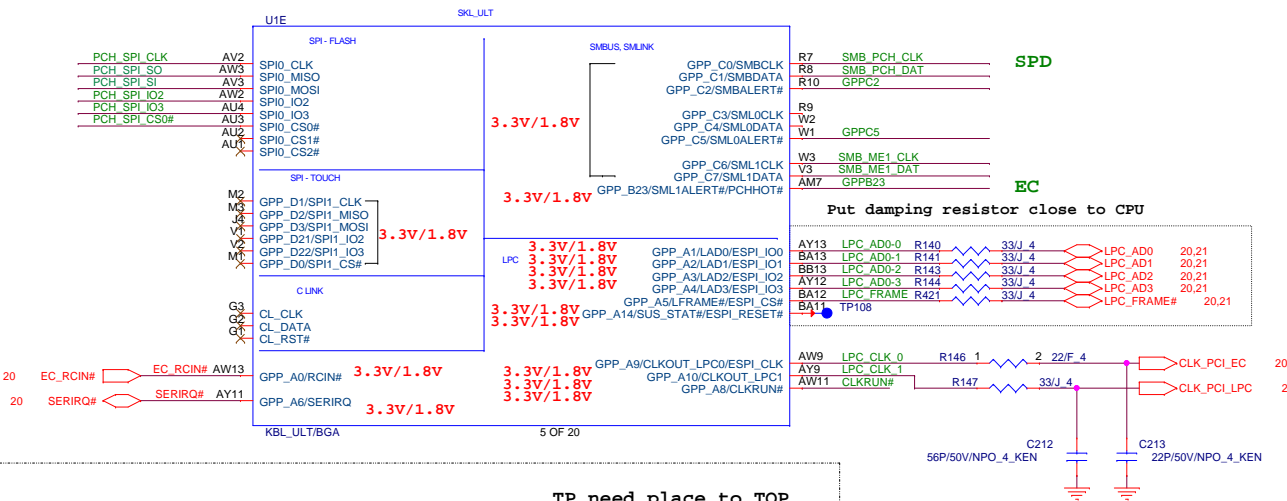
# KabyLake ULT (HDA/SDXC)

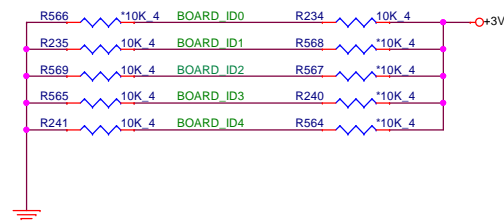
GPPC5: ESPI or LPC SEL  
HIGH: ESPI interface  
LOW: LPC interface(default)INT DN

11



## KabyLake ULT (LPC/SPI/SMB/CLINK)





**PANEL ID**

PANEL ID	
H	HD
I	FHD

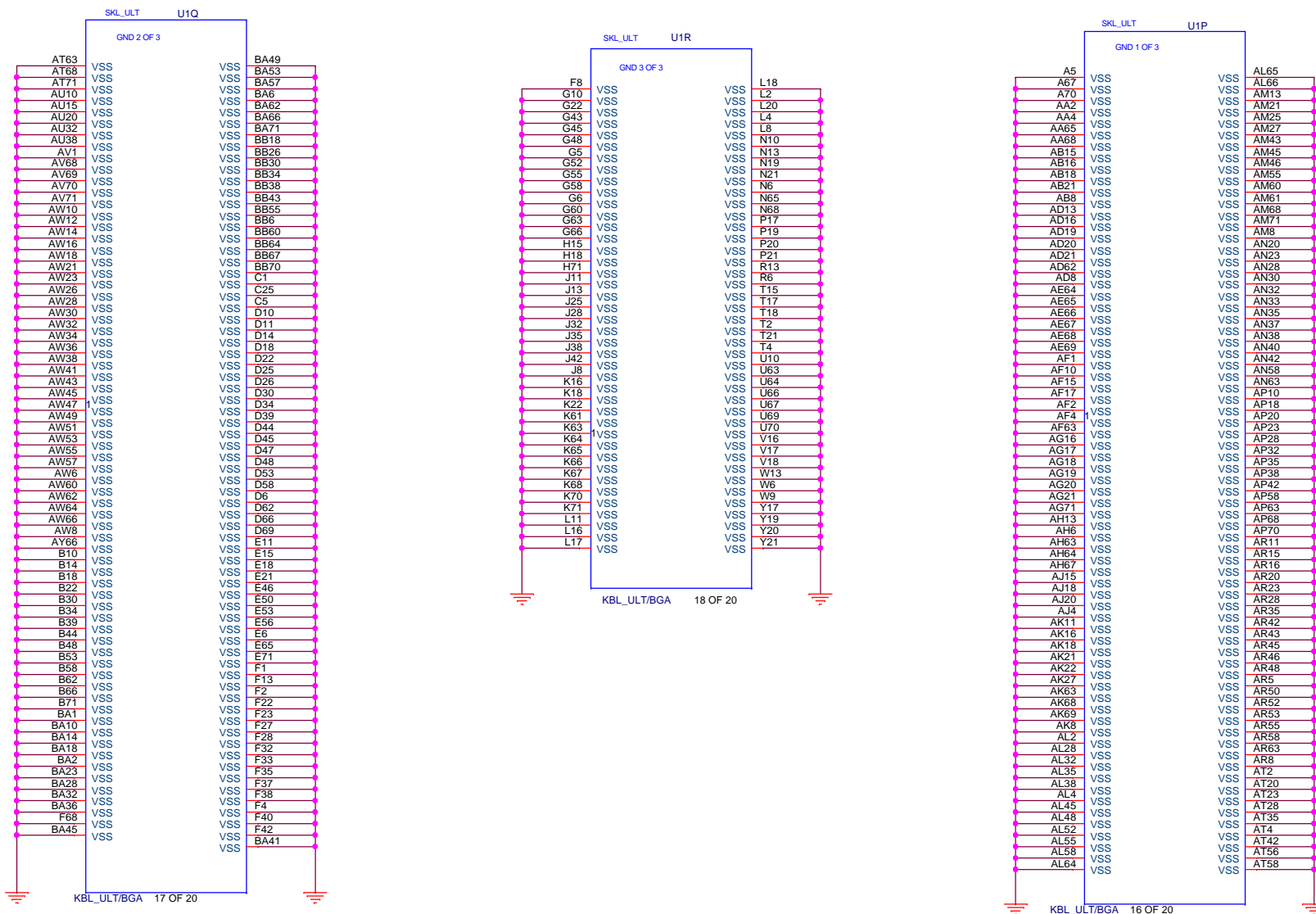
GPP_B22(Boot BIOS)	
PU	LPC
PD	SPI (Default IPD)

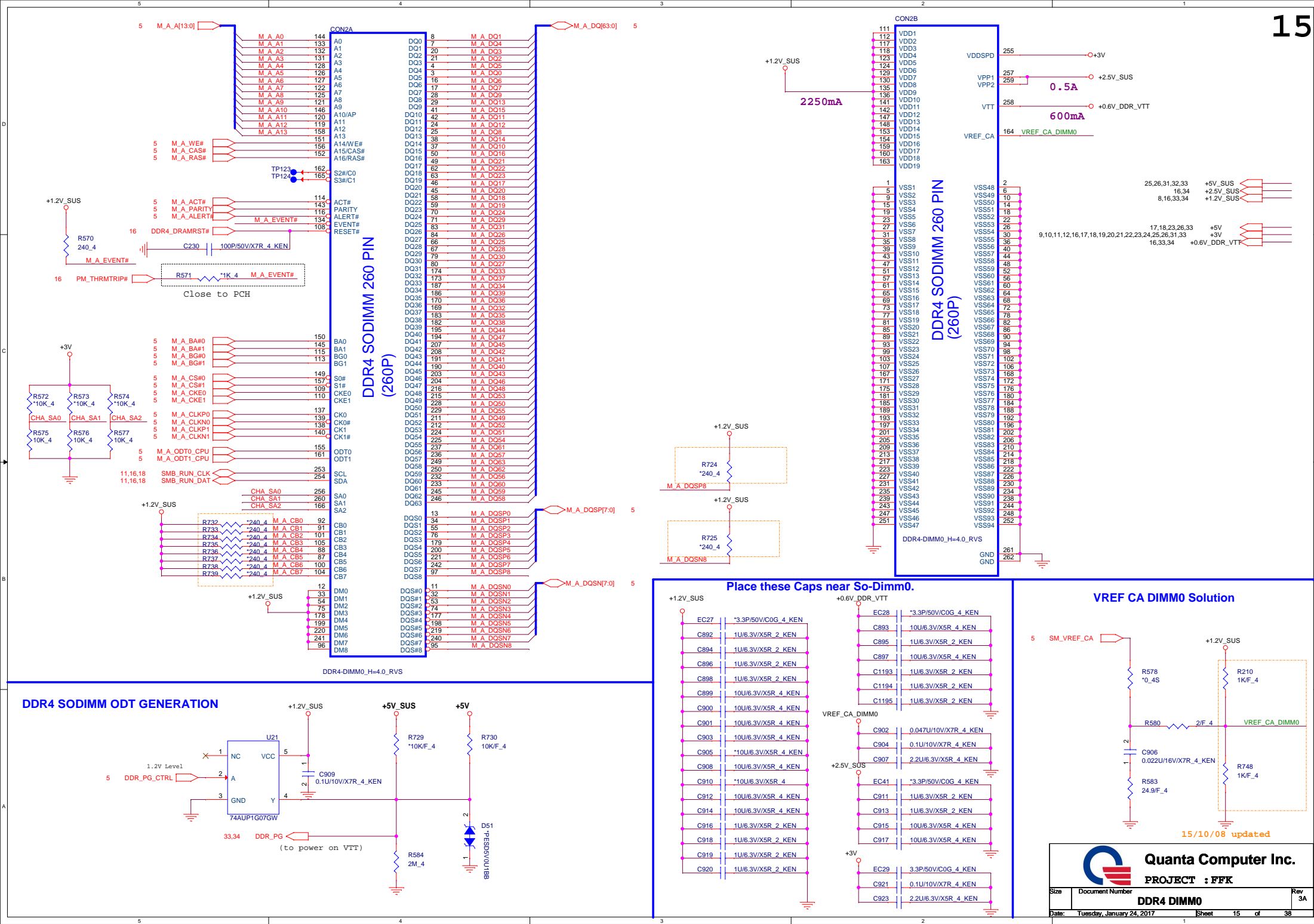
  

No Reboot Strap(GPP_B18)	
NC	Default
PU	EN

[illegible]



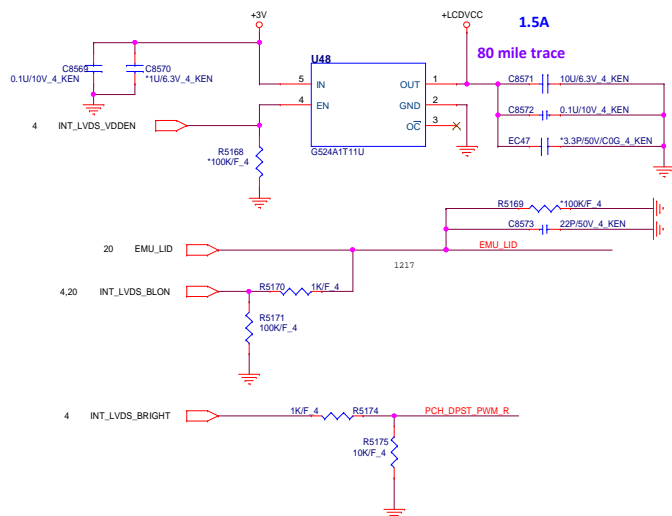




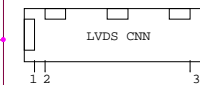
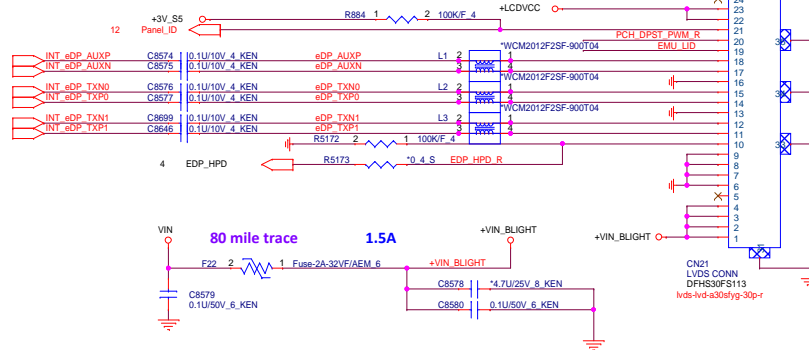






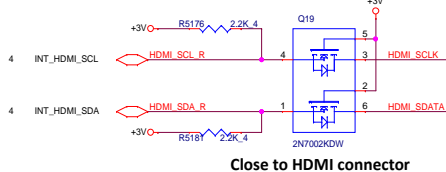


USB CAMERA  
D\_MIC



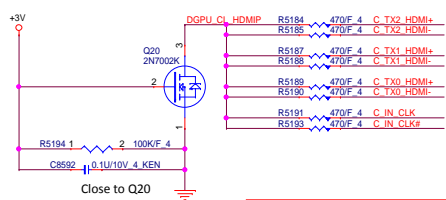
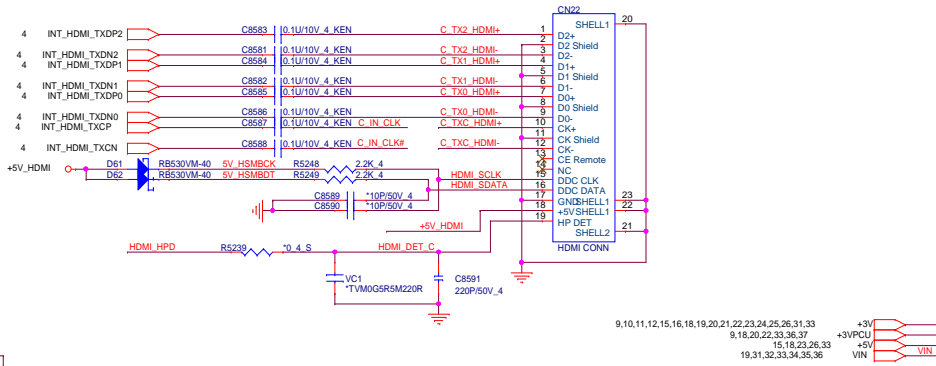
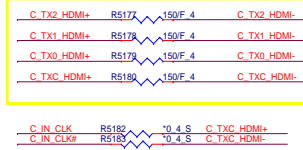
HDMI Conn.

HDMI SMBus Isolation

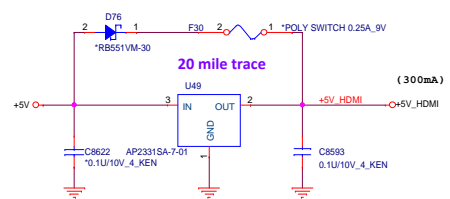
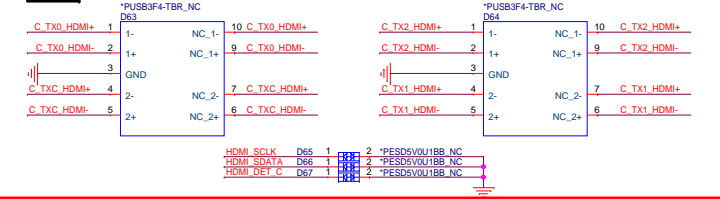


Close to HDMI connector

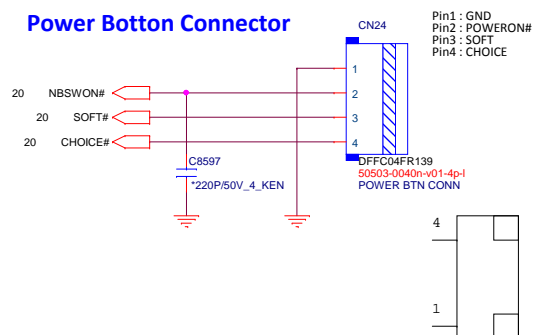
EMI Solution



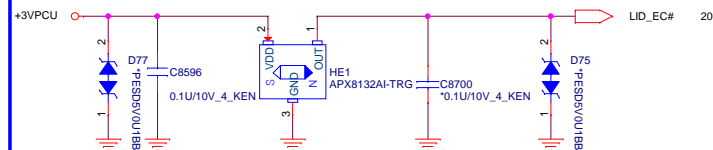
ESD



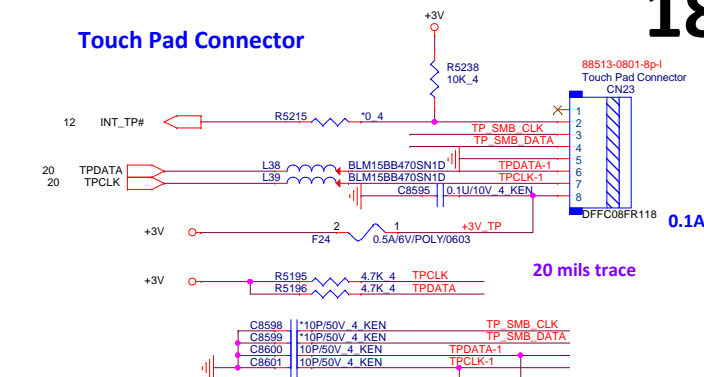
## Power Button Connector



## HALL SENSOR



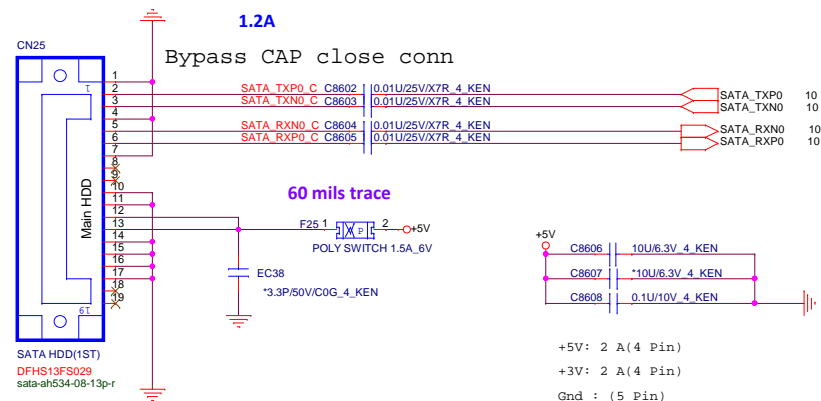
## Touch Pad Connector



20 mils trace

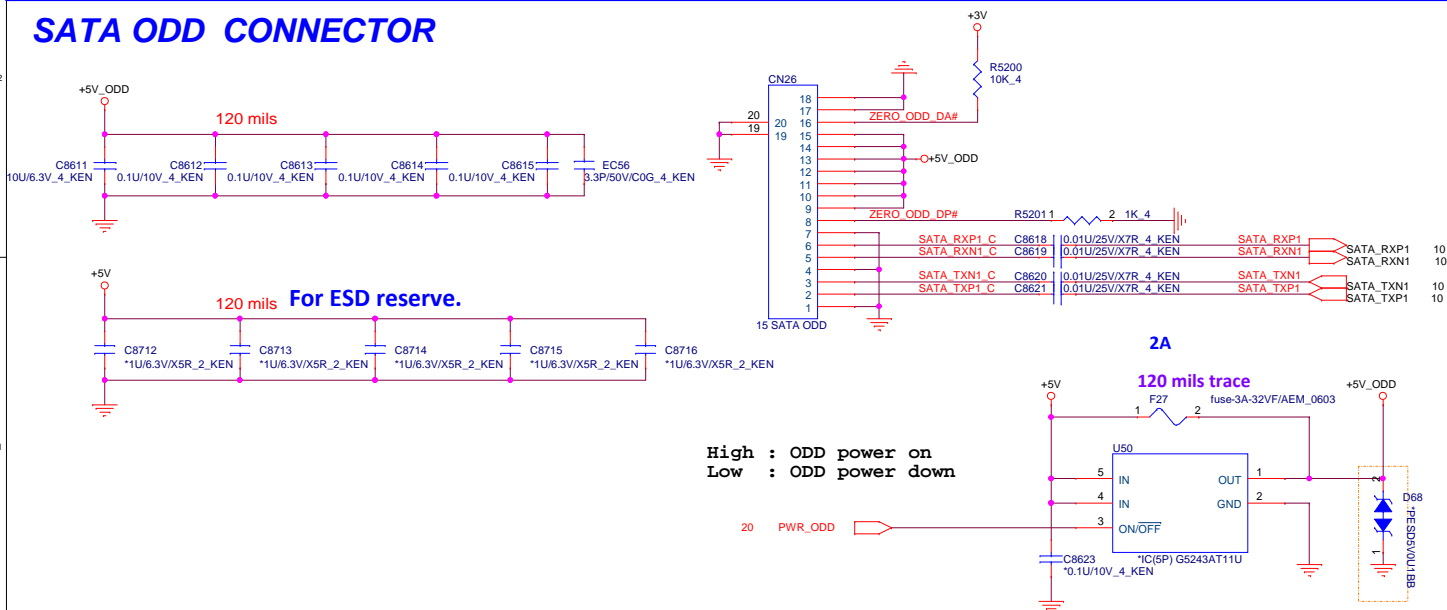
0.1A

## SATA HDD Connector(Cable type)



60 mils trace

## SATA ODD CONNECTOR

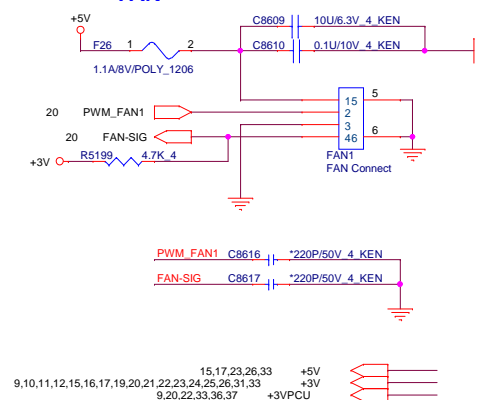


High : ODD power on  
Low : ODD power down

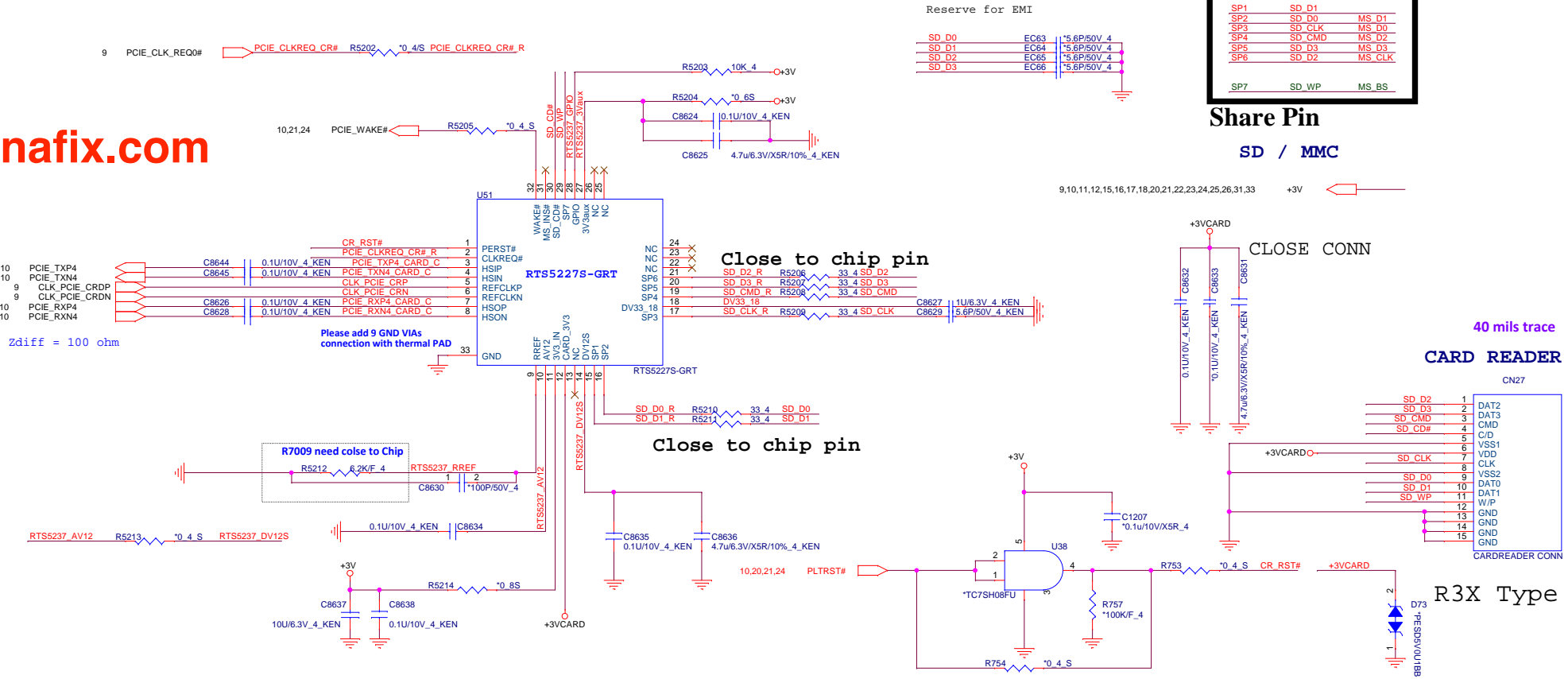
2A

120 mils trace

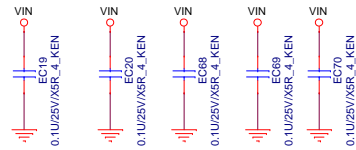
## FAN

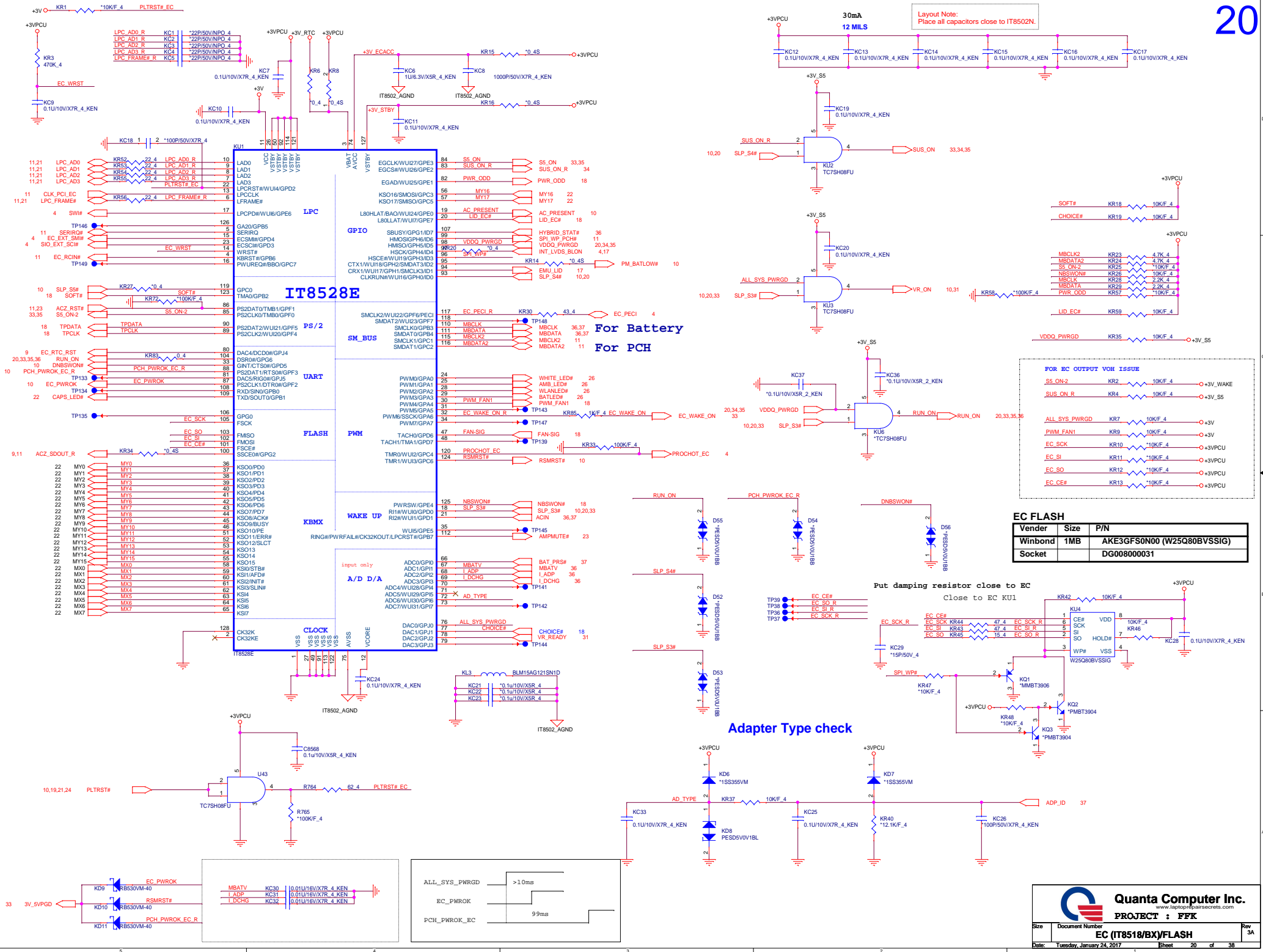


Vinafix.com



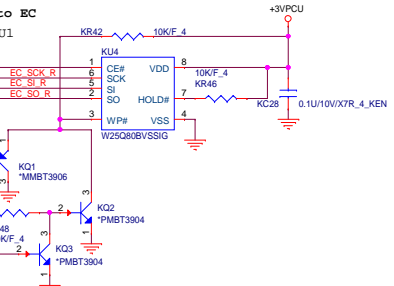
EMI



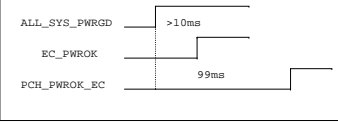
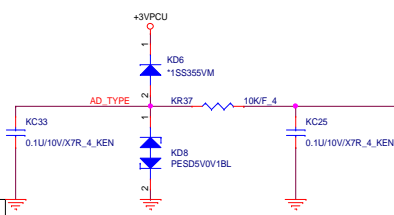


**EC FLASH**

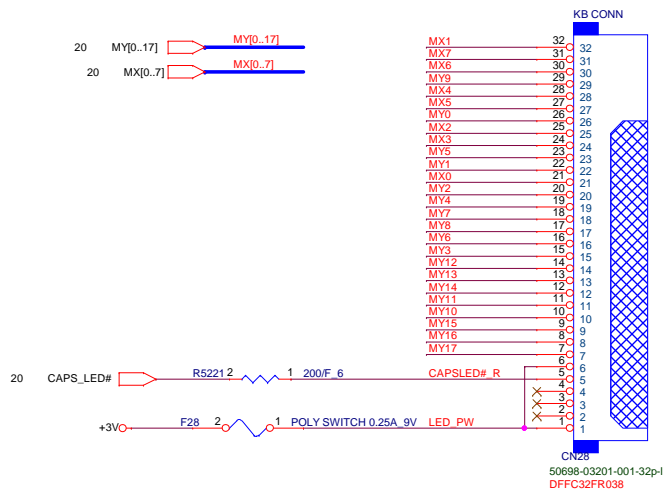
Vender	Size	P/N
Winbond	1MB	AKE3GF50N00 (W25Q80BVSSIG)
Socket		DG008000031



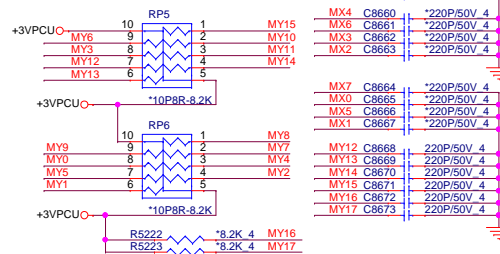
Adapter Type check





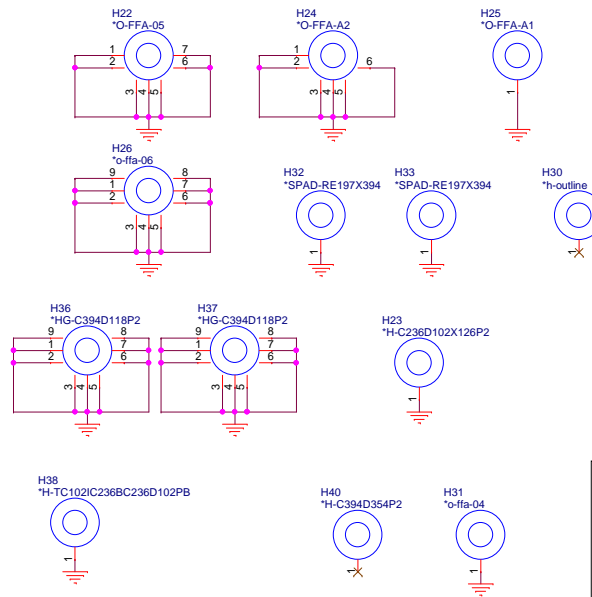


KEYBOARD PULL-UP

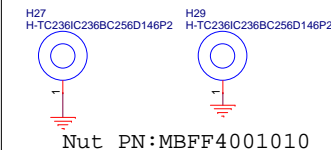


Hole

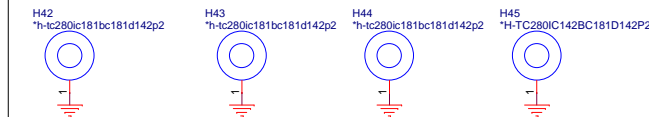
9,10,11,12,15,16,17,18,19,20,21,23,24,25,26,31,33  
+3VPCU  
+3V



FAN nut



CPU BLK

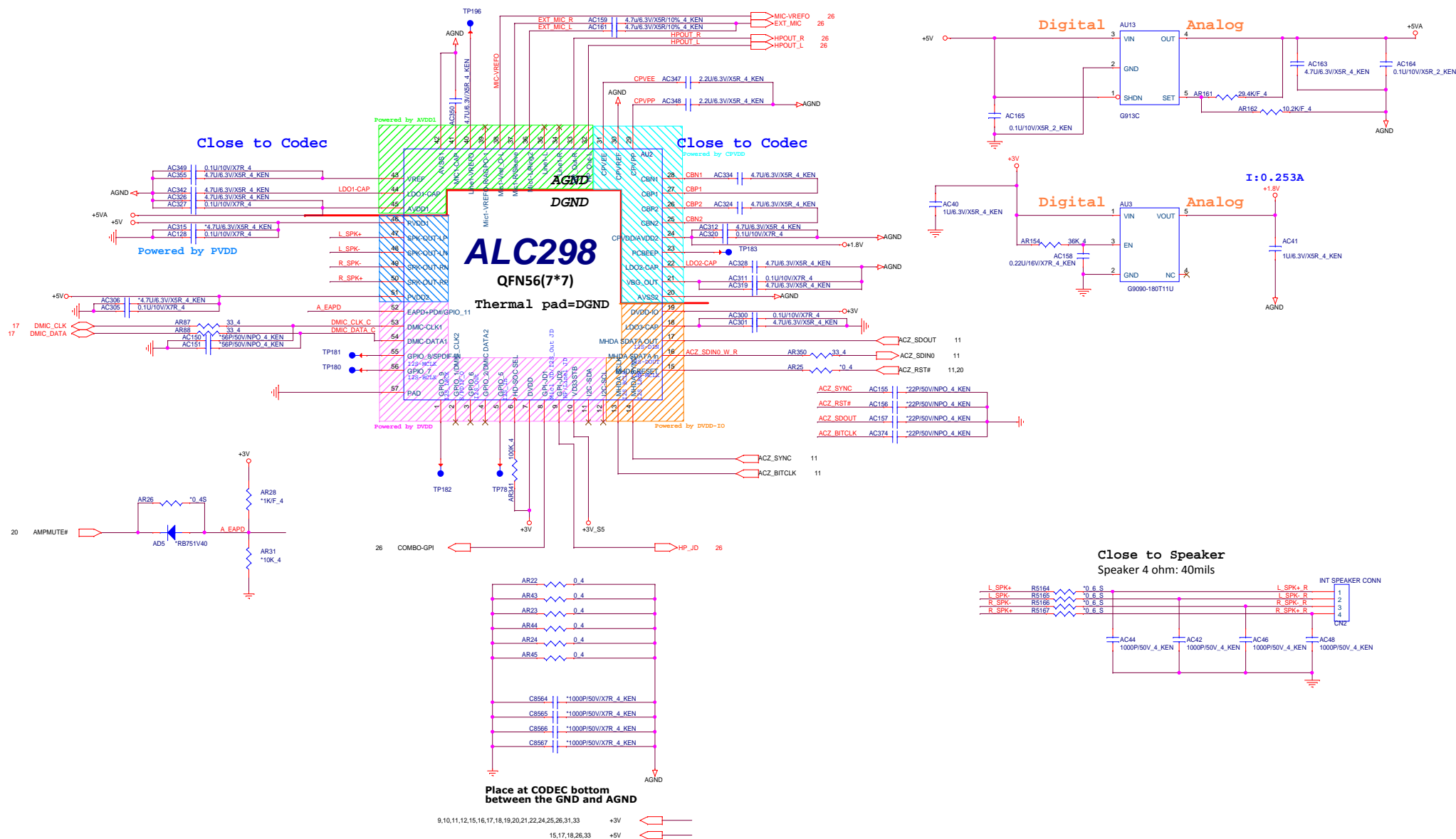


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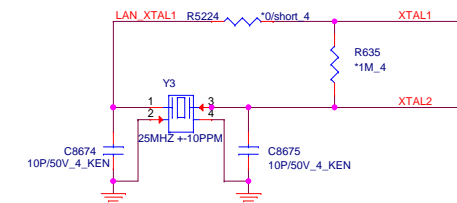
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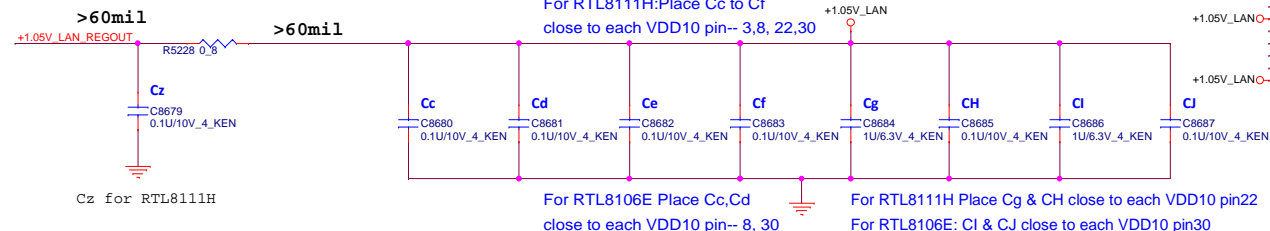
**AUDIO(ALC298-VA0-CG)**



```
if ISOLATEB pin
pull-low, the LAN
chip will not drive
it's PCI-E outputs
( excluding
PCIE_WAKE# pin )
```



For RTL8111H:Place Cc to Cf  
close to each VDD10 pin-- 3,8, 22,30

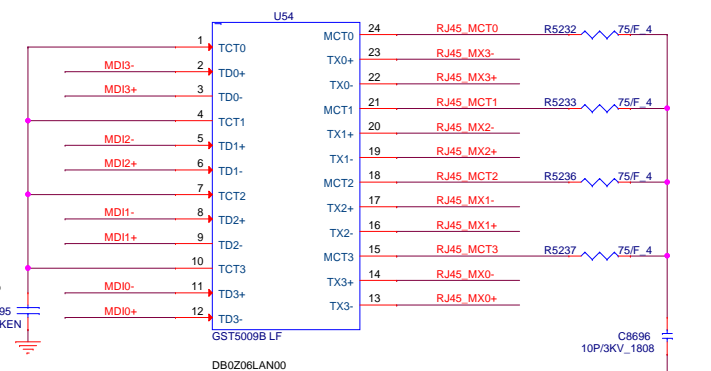
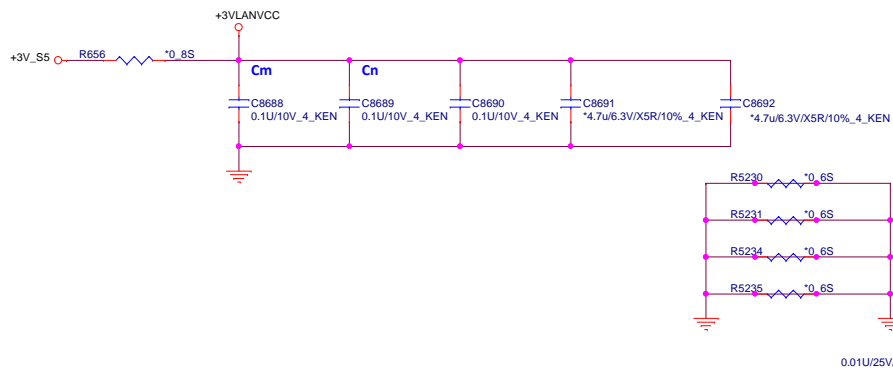


	R5228	Cz C8679
RTL8111H	Add	Add
RTL8106E	NC	NC

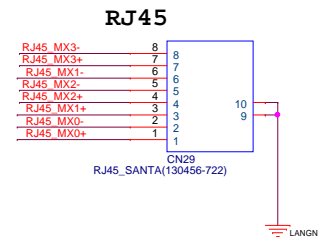
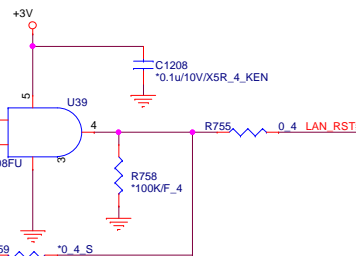
For RTL8111H :

- \*Place Cm and Cn close to each VDD33 pin-- 11, 32
- \*For surge improvement place C8691 and C8692 close to each VDD33 pin-- 11, 32. (optional)

For RTL8106E : Place Cn and C8690 close to each VDD33 pin-- 23, 32



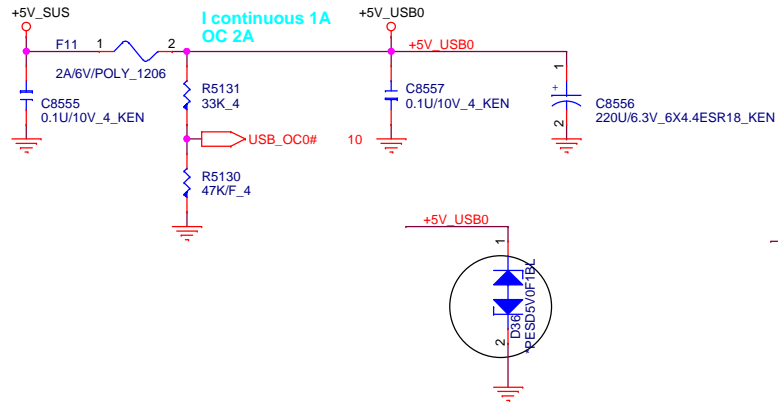
1000: DB0Z06LAN00  
10/100: DB0EL5LAN00



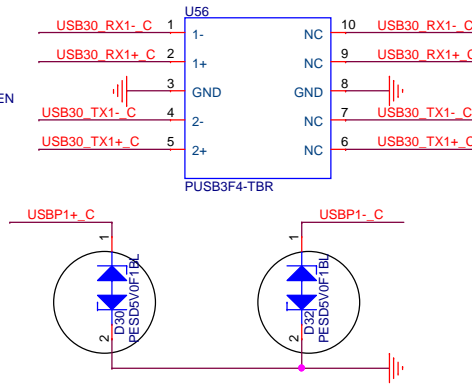


# USB 2.0/3.0 Combo

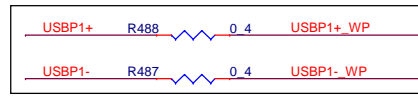
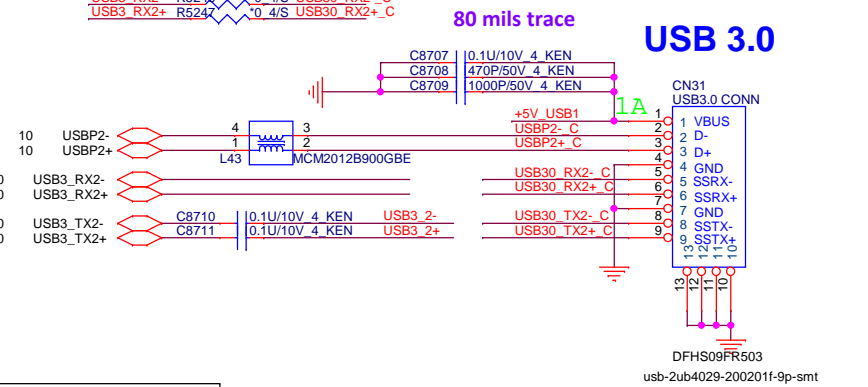
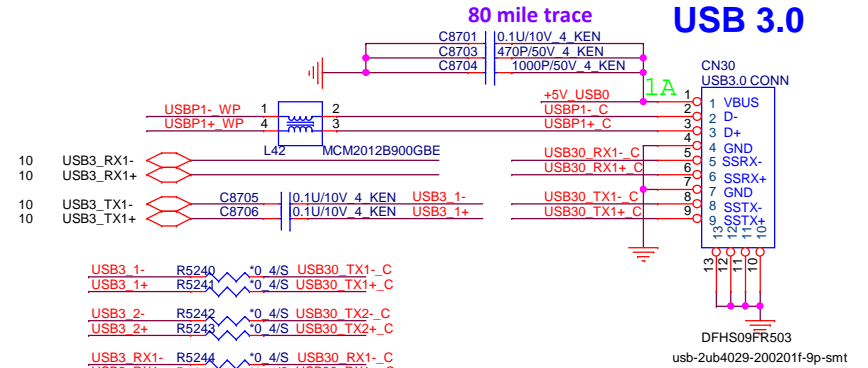
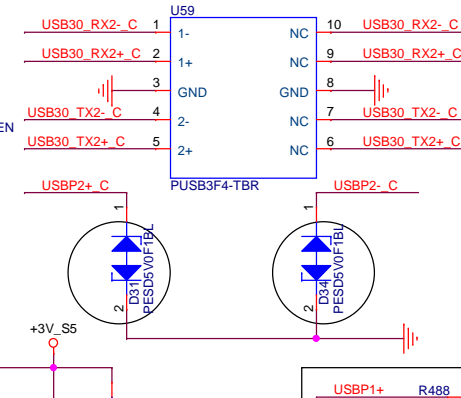
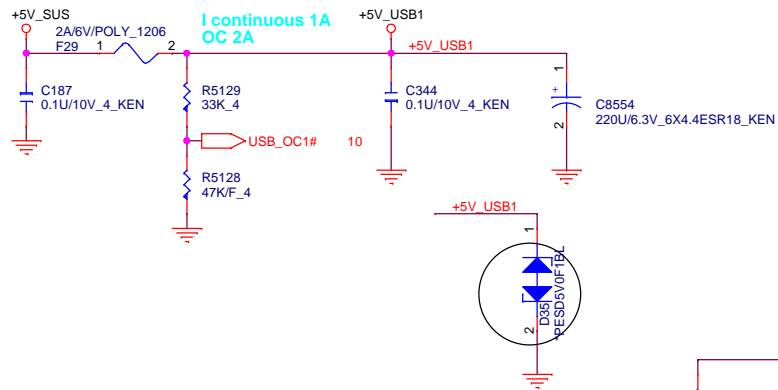
## USB OCP



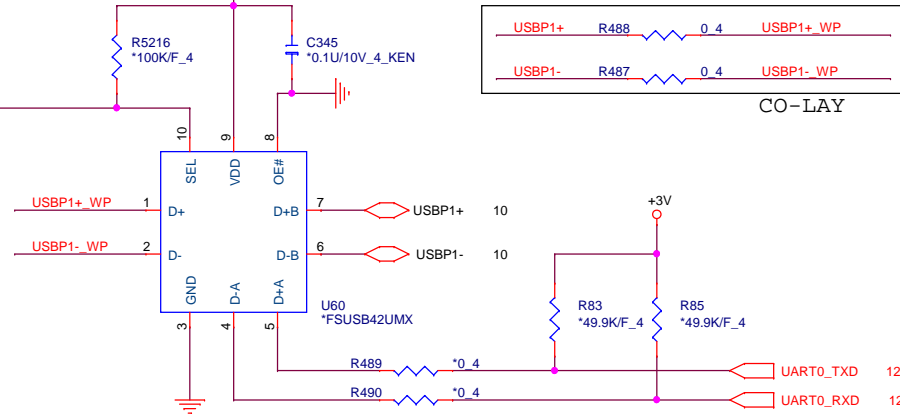
## ESD



## USB OCP



/OE	SEL	Function
H	X	I/O=Hi-z
L	L	D(+/-) to D(+/-)A
L	H	D(+/-) to D(+/-)B



9,18,20,22,33,36,37  
15,26,31,32,33

+3VPCU  
+5V\_SUS



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5 4 3 2 1

D

C

B

A

5 4 3 2

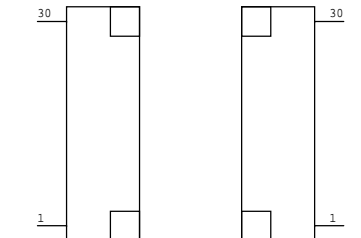
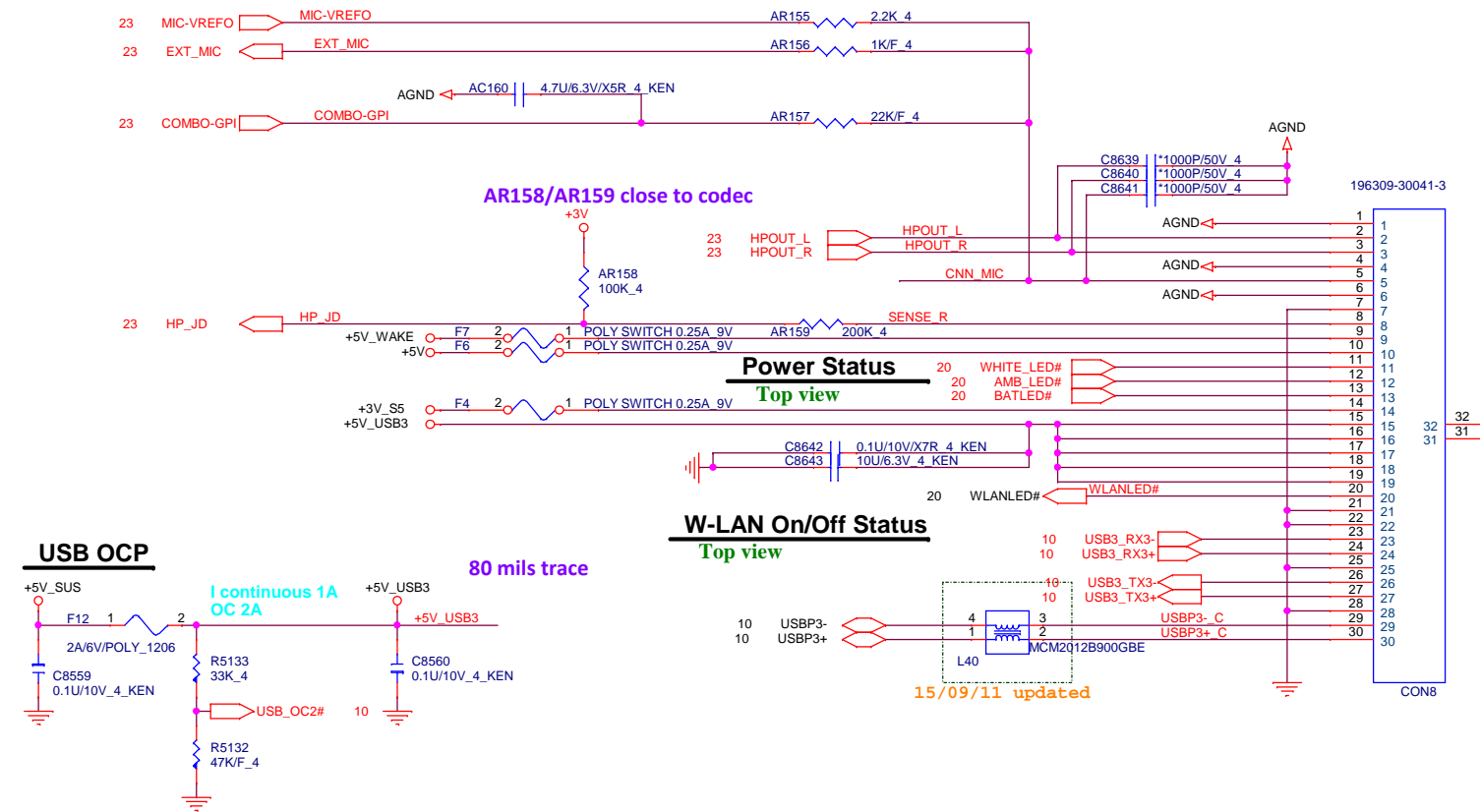
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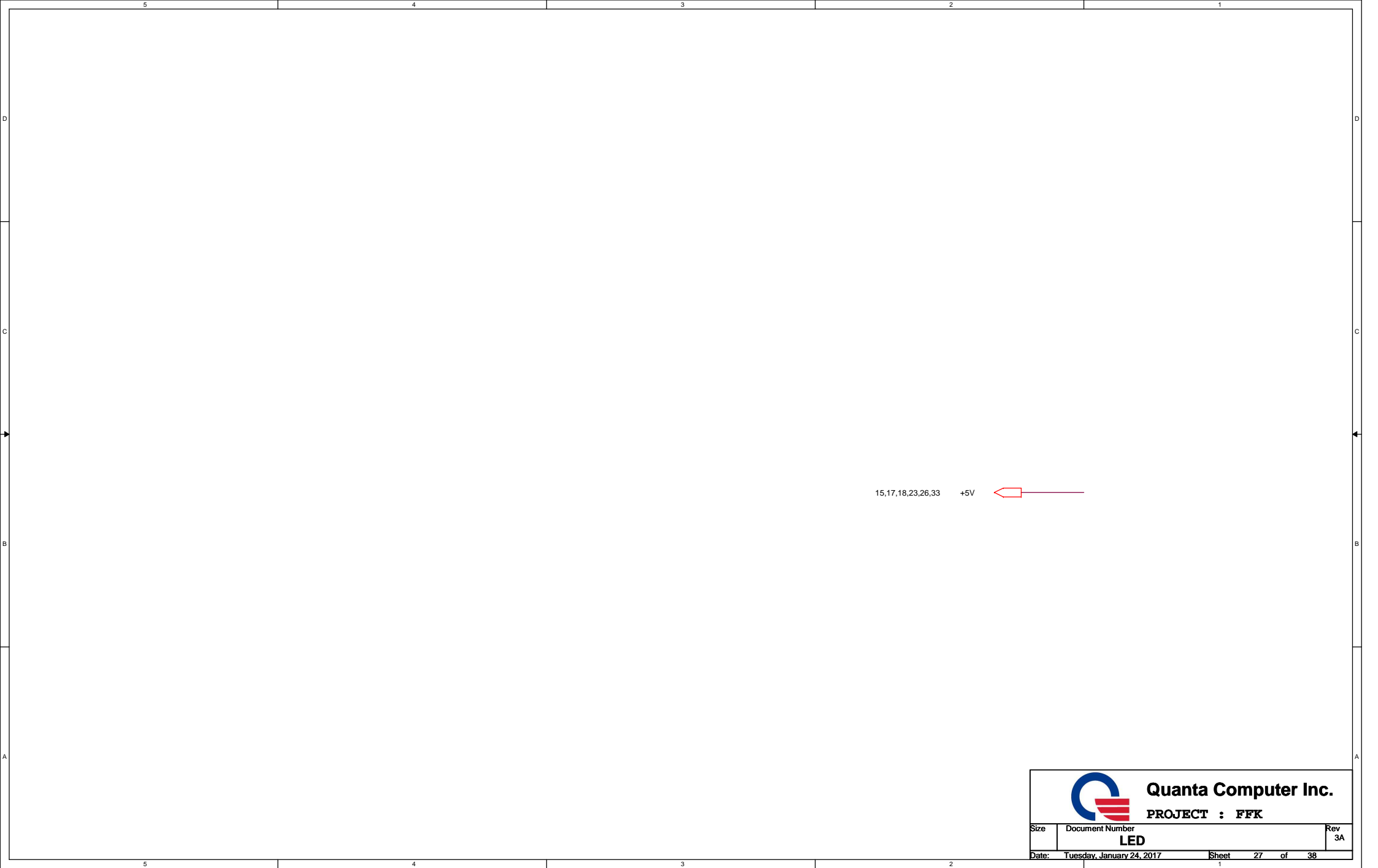
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- 9,18,20,22,33,36,37
- 15,25,31,32,33
- 9,10,11,12,15,16,17,18,19,20,21,22,23,24,25,31,33
- 33,34,35
- 4,9,10,11,13,17,20,21,23,24,25,33,34
- +3VPCU
- +5V\_SUS
- +3V
- +5V\_WAKE
- +3V\_S5

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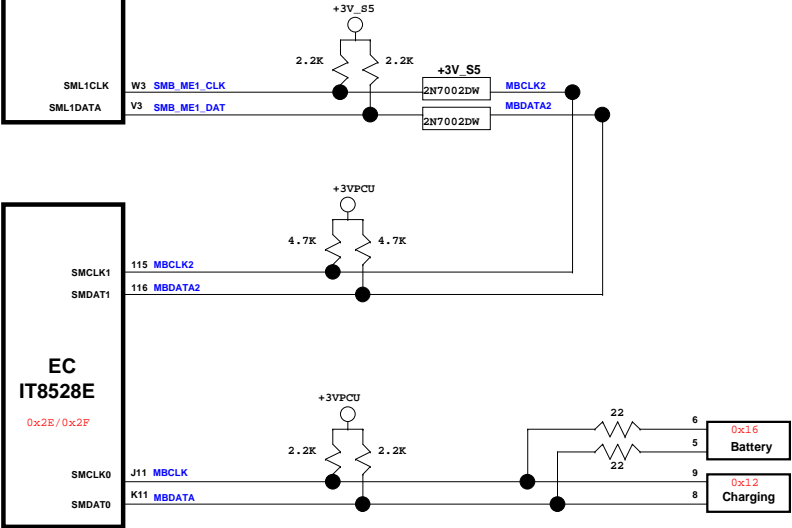
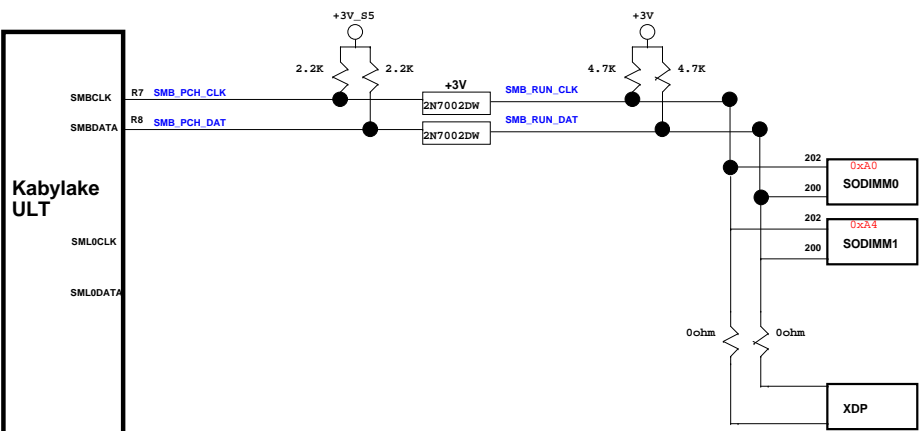


OS status	S0	S3		(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)
H/W status	S0	S3		S4 (Win8 off) RTC wake Enable WOLAN Enable	S4 (Win8 off) RTC wake Disable WOLAN Disable	S5 Charge Enable	S5 Charge Disable WoL Disable	S5 WoL Enable
RUN_ON	H	L		L	L	L	L	L
+3V	H	L		L	L	L	L	L
+5V	H	L		L	L	L	L	L
+0.6V_DDR_VTT	H	L		L	L	L	L	L
+VCCSA	H	L		L	L	L	L	L
+VCC_GFX	H	L		L	L	L	L	L
+VCC_CORE	H	L		L	L	L	L	L
+1.0V_VCCIO(+1.0V_VCCSTG)	H	L		L	L	L	L	L
SUS_ON	H	H		L	L	L	L	L
+5V_SUS	H	H		L	L	L	L	L
+1.2V_SUS	H	H		L	L	L	L	L
S5_ON	H	H		H	L	L	L	H
+3V_S5	H	H		H	L	L	L	H
+1.0V_S5	H	H		H	L	L	L	H
EC_WAKE_ON	H	H		H	L	H	L	H
+3V_WAKE	H	H		H	L	H	L	H
+5V_WAKE	H	H		H	L	H	L	H

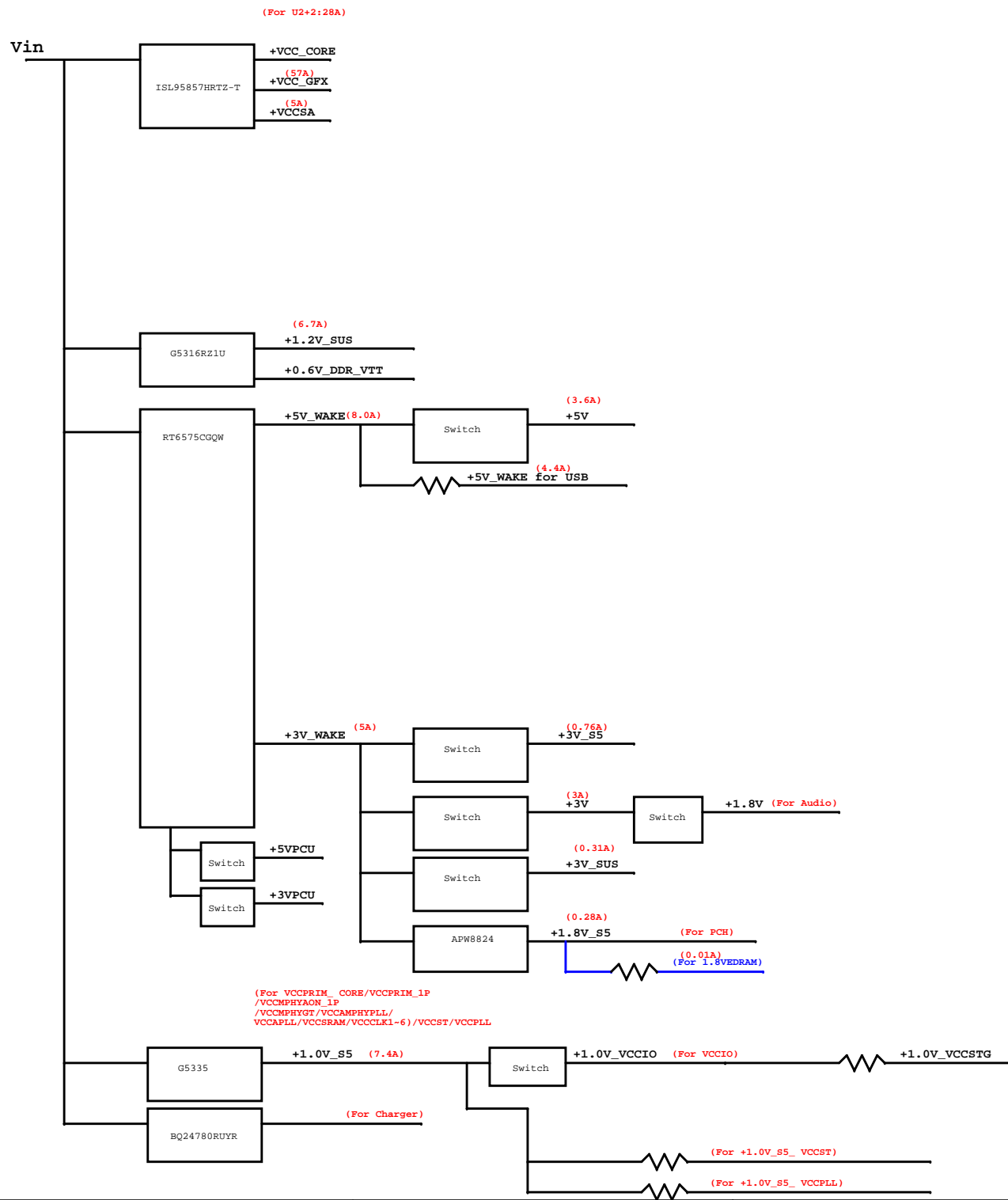
(+1.0V\_S5:For VCCPRIM\_CORE/VCCPRIM\_1P  
/VCCMPHYAON\_1P  
/VCCMPHYGT/VCCAMPHYPLL/  
VCCAPLL/VCCSRAM/VCCCLK1~6)/VCCST/VCCPLL

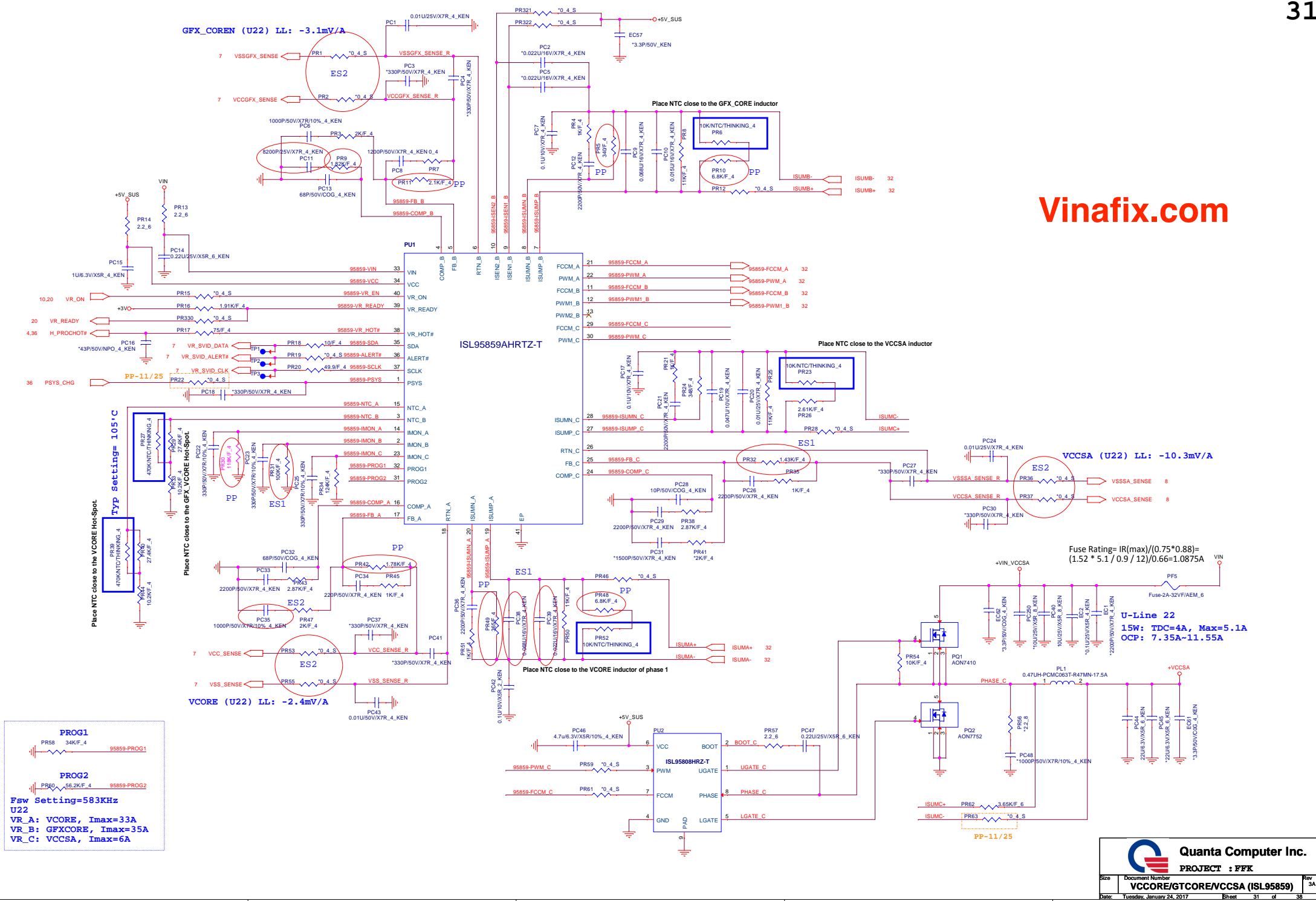
Resister tolerance:  
F :+/- 1%, (example:69.8K/F\_4)  
others are +/- 5%, (example:69.8K\_4)  
Capacitor tolerance:  
X7R: +/- 10%  
X5R: +/- 10%  
Y5V: +80%~-20%  
others are +/- 5%

 <b>Quanta Computer Inc.</b> <b>PROJECT : FFK</b>		Size	Document Number	Rev
		<b>POWER MAP</b>		3A
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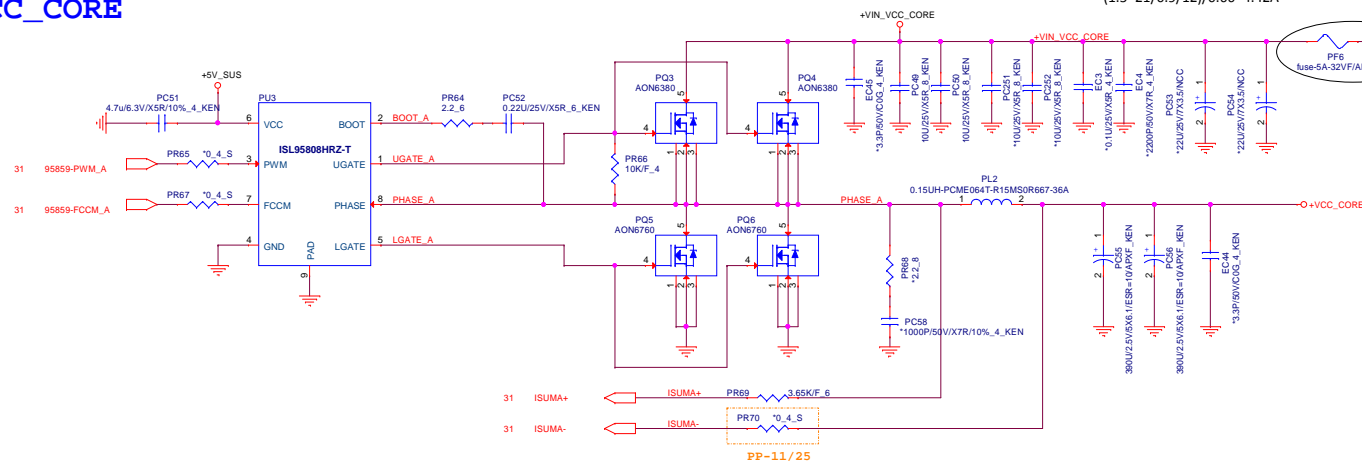


Function	IC	SMBus Address
Thermal IC	NCT7717U	1001000xb (0x90)
Charge IC	ISL88732HRTZ-T	TBD
Battery	Battery	TBD
NFC	TBD	TBD

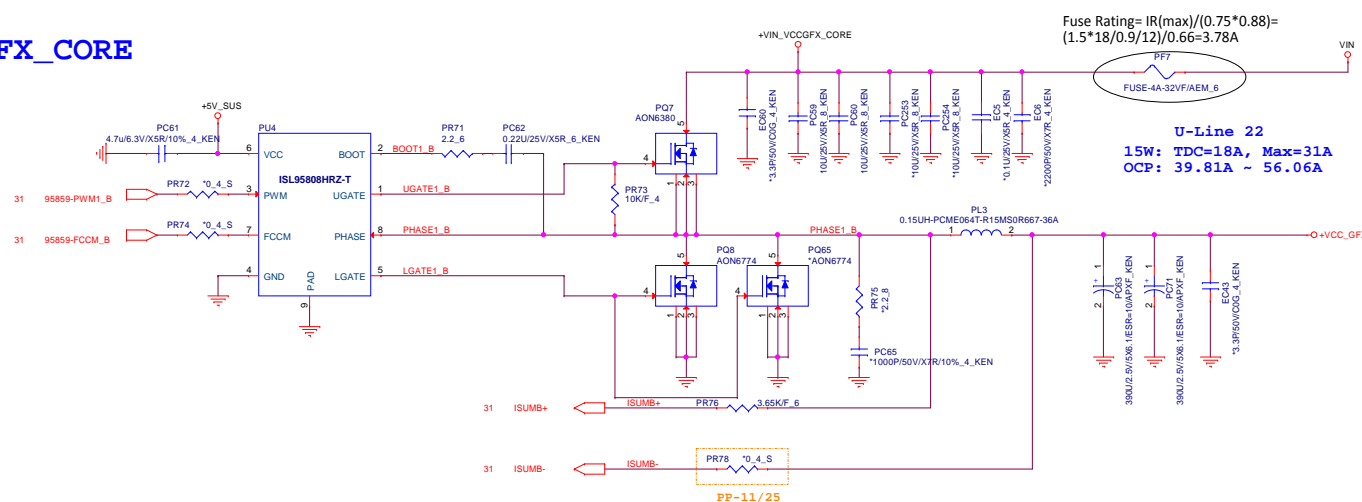




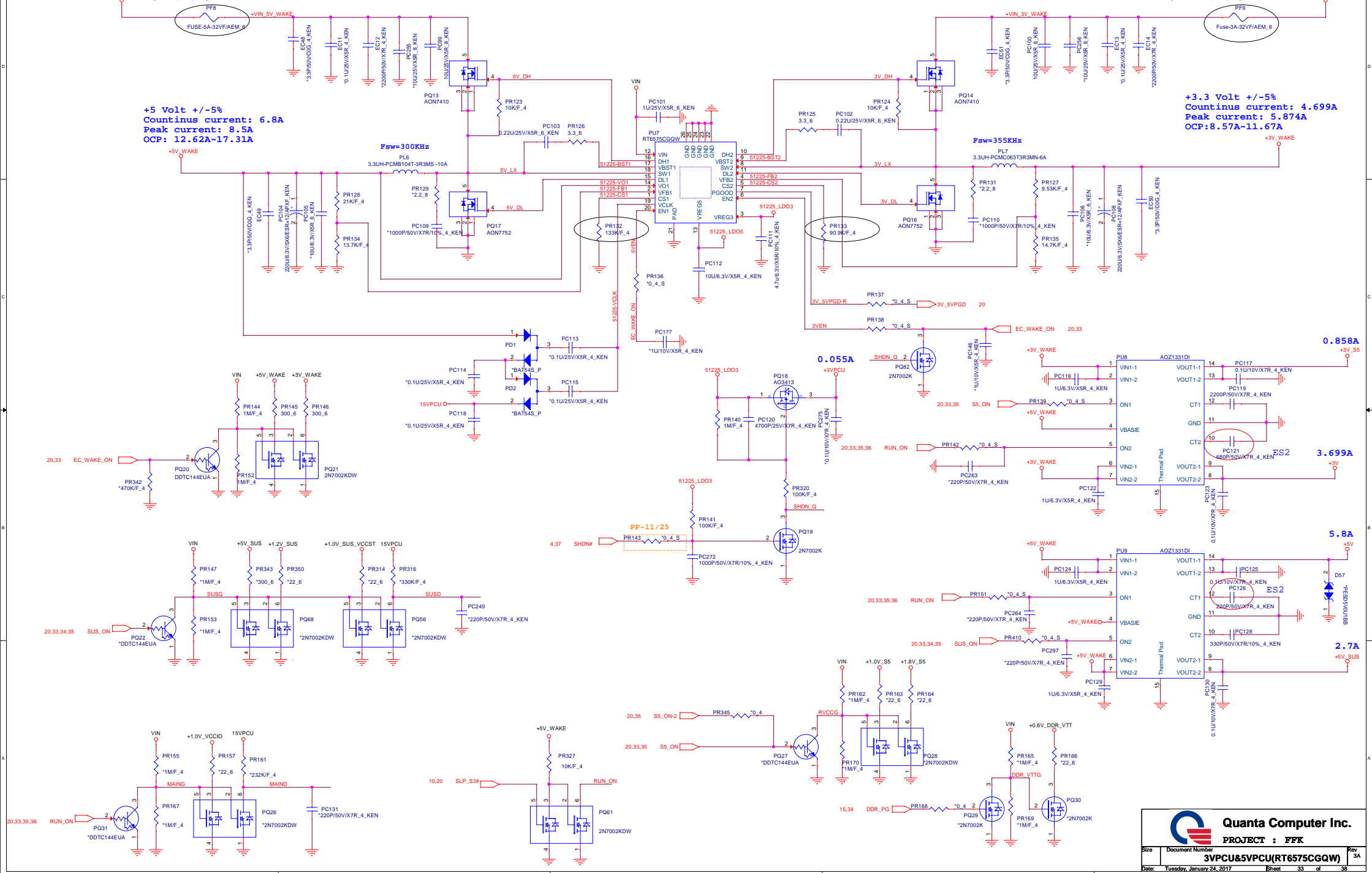
## GFX\_CORE



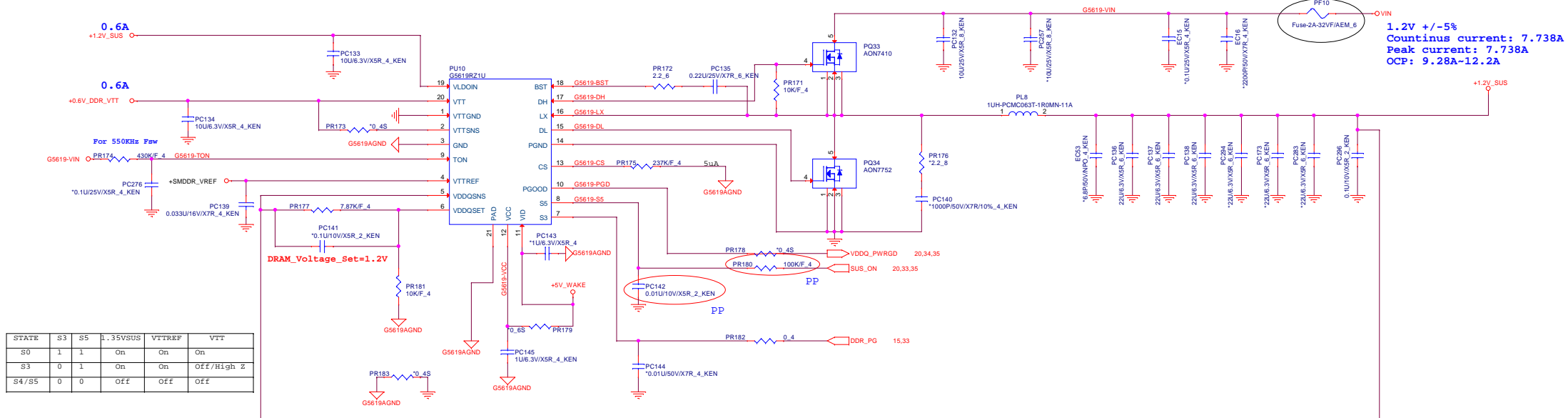
U-Line 22  
15W: TDC=21A, Max=32A  
OCP: 43.94A ~ 60.18A



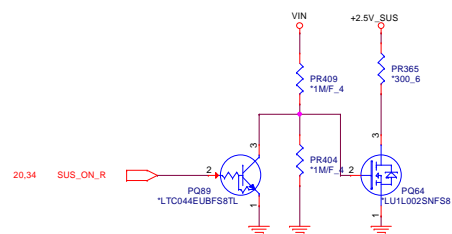
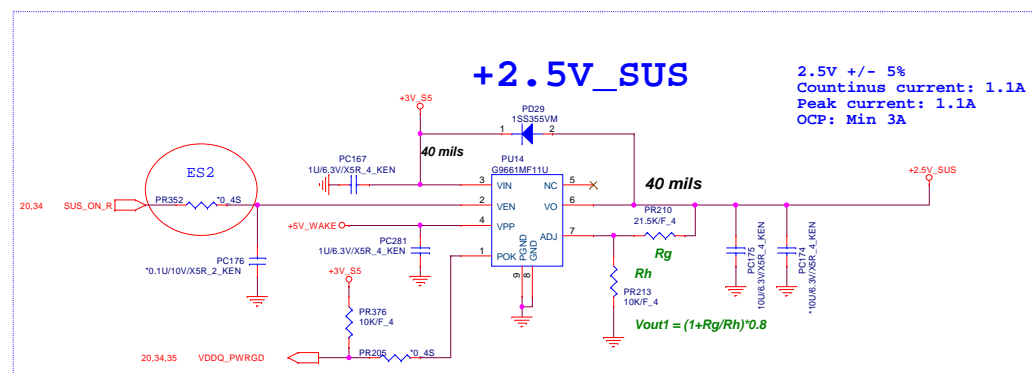


$$\text{Fuse Rating} = I_R(\max) / (0.75 * 0.88) = (3.3 * 4.699 / 0.9 / 12) / 0.66 = 2.175 \text{ A}$$


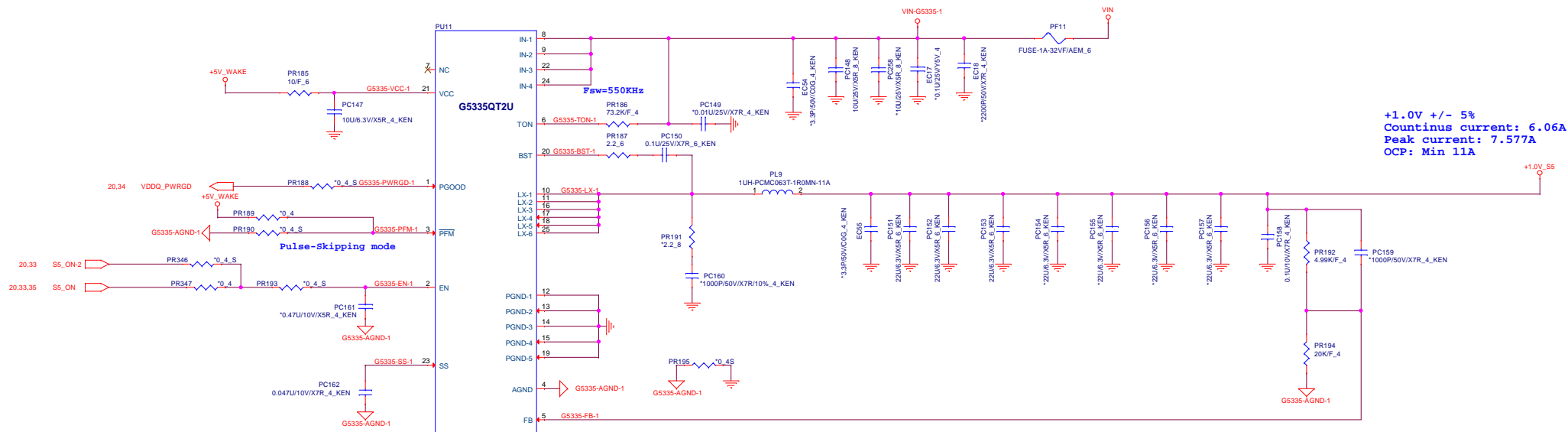
## 1.2VSUS & VTT MEM

$$\text{Fuse Rating} = I_R(\text{max}) / (0.75 * 0.88) = (1.2 * 7.738 / 0.9 / 12) / 0.66 = 1.3026 \text{ A}$$


STATE	S3	S5	1.35VSUS	VITREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	0	0	Off	Off	Off

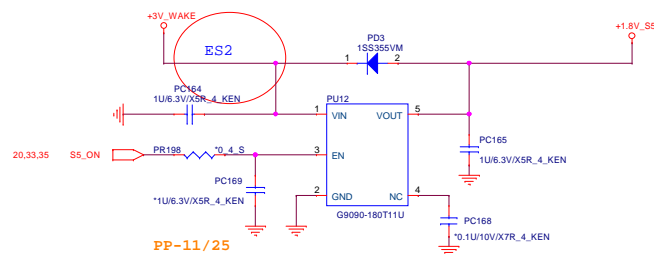


+1.0V\_S5

$$\text{Fuse Rating} = I_R(\text{max}) / (0.75 * 0.75) = (1.0 * 6.06 / 0.9 / 12) / 0.66 = 0.85 \text{ A}$$


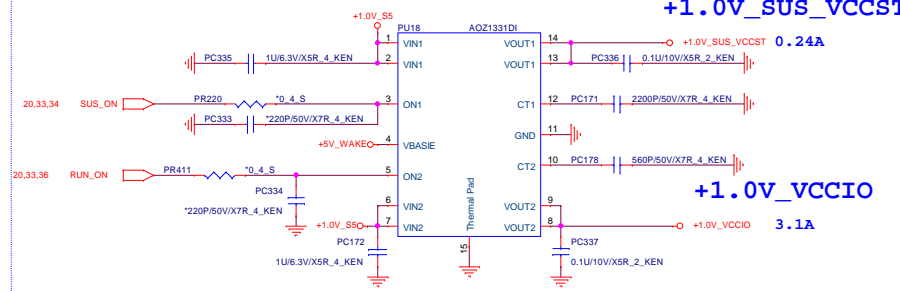
+1.8V\_S5

1.8V +/- 5%  
Countinus current: 0.217A  
Peak current: 0.217A



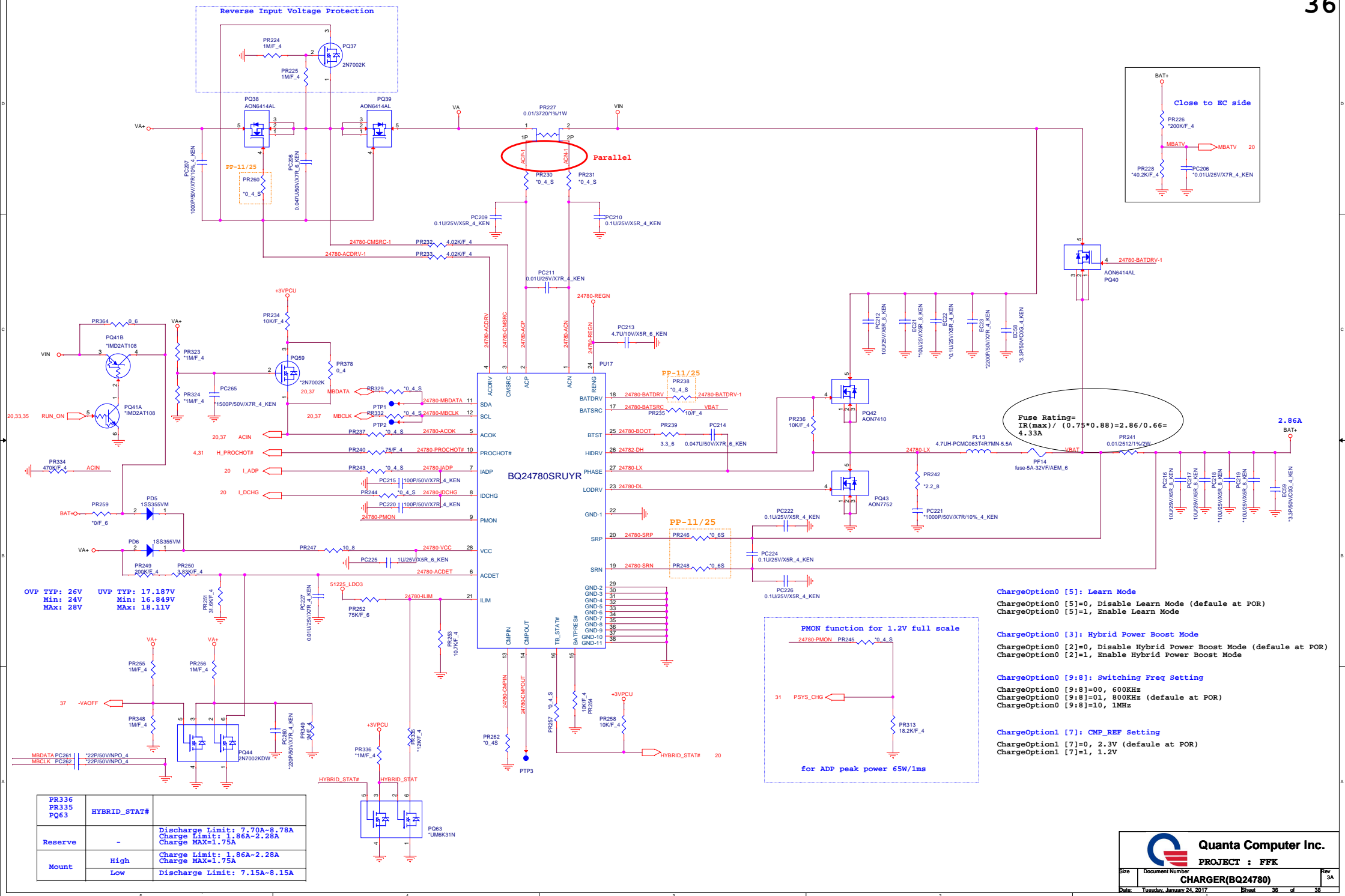
## +1.0V\_SUS\_VCCST

+1.0V\_SUS\_VCCST 0.24A



+1.0V\_VCCIO

+1.0V\_VCCIO 3.1A



Fuse Rating=  
 $IR(\max) / (0.75 \times 0.88) = 2.25 / 0.66 = 3.409A$

The diagram shows an adapter discharge circuit. An AC input (ACIN) is connected to a network of resistors (PR217, PR297, PR295, PR299, PR293, PR296, PR294, PR292). A diode (PD21) is connected to the network. A MOSFET (PD22) is connected to the network and a capacitor (C2). The output is labeled -VADIFF and -VADIFF. The circuit is powered by VDD and GND.

The schematic diagram illustrates the power management section of the T1020, featuring several voltage regulators and MOSFETs. The diagram is organized into sections for different power rails:

- +VCC\_CORE:** Includes the PQ3, PQ4, PQ5, and PQ6 MOSFETs, along with the PC232 capacitor and the 51225\_LDO3 voltage regulator.
- +VCC\_WAKE:** Includes the PQ1, PQ2 MOSFETs, the PC232 capacitor, and the 51225\_LDO3 voltage regulator.
- +VCC\_GFX:** Includes the PQ7, PQ8, and PQ65 MOSFETs, the PC232 capacitor, and the 51225\_LDO3 voltage regulator.
- +VCC\_CPU:** Includes the PQ14, PQ16 MOSFETs, the PC232 capacitor, and the 51225\_LDO3 voltage regulator.
- +VCC\_SUS:** Includes the PQ13, PQ17 MOSFETs, the PC232 capacitor, and the 51225\_LDO3 voltage regulator.
- +VCC\_WAKE (ADP IN):** Includes the PQ38, PQ39 MOSFETs, the PC232 capacitor, and the 51225\_LDO3 voltage regulator.
- +VCC\_WAKE (BATT IN):** Includes the PQ40 MOSFET, the PC232 capacitor, and the 51225\_LDO3 voltage regulator.
- +VCC\_CPU (Charge):** Includes the PQ42, PQ43 MOSFETs, the PC232 capacitor, and the 51225\_LDO3 voltage regulator.

Key components and their values are as follows:

- Resistors:** PR263 (100K), PR264 (4.87K), PR267 (12K), PR268 (12K), PR269 (12K), PR270 (12K), PR271 (12K), PR272 (300K), PR273 (100K), PR274 (10K), PR275 (10K), PR276 (10K), PR277 (10K), PR278 (10K), PR279 (10K), PR280 (10K), PR281 (10K), PR282 (10K), PR283 (10K), PR284 (10K), PR285 (10K), PR286 (10K), PR287 (10K), PR288 (10K), PR289 (10K), PR290 (10K), PR291 (10K), PR292 (10K), PR293 (10K), PR294 (10K), PR295 (10K), PR296 (10K), PR297 (10K), PR298 (10K), PR299 (10K), PR300 (10K).
- Capacitors:** PC232 (0.1uF), PC233 (10uF), PC234 (10uF), PC235 (10uF), PC236 (10uF), PC237 (10uF), PC238 (10uF), PC239 (10uF), PC240 (10uF), PC241 (10uF), PC242 (10uF), PC243 (10uF), PC244 (10uF), PC245 (10uF), PC246 (10uF), PC247 (10uF), PC248 (10uF), PC249 (10uF), PC250 (10uF), PC251 (10uF), PC252 (10uF), PC253 (10uF), PC254 (10uF), PC255 (10uF), PC256 (10uF), PC257 (10uF), PC258 (10uF), PC259 (10uF), PC260 (10uF), PC261 (10uF), PC262 (10uF), PC263 (10uF), PC264 (10uF), PC265 (10uF), PC266 (10uF), PC267 (10uF), PC268 (10uF), PC269 (10uF), PC270 (10uF), PC271 (10uF), PC272 (10uF), PC273 (10uF), PC274 (10uF), PC275 (10uF), PC276 (10uF), PC277 (10uF), PC278 (10uF), PC279 (10uF), PC280 (10uF), PC281 (10uF), PC282 (10uF), PC283 (10uF), PC284 (10uF), PC285 (10uF), PC286 (10uF), PC287 (10uF), PC288 (10uF), PC289 (10uF), PC290 (10uF), PC291 (10uF), PC292 (10uF), PC293 (10uF), PC294 (10uF), PC295 (10uF), PC296 (10uF), PC297 (10uF), PC298 (10uF), PC299 (10uF), PC300 (10uF).
- MOSFETs:** PQ47 (PM873005), PQ48 (2N7002K), PQ49 (2N7002K), PQ50 (2N7002K), PQ51 (2N7002K), PQ52 (2N7002K), PQ53 (2N7002K), PQ54 (2N7002K), PQ55 (2N7002K), PQ56 (2N7002K), PQ57 (2N7002K), PQ58 (2N7002K), PQ59 (2N7002K), PQ60 (2N7002K), PQ61 (2N7002K), PQ62 (2N7002K), PQ63 (2N7002K), PQ64 (2N7002K), PQ65 (2N7002K), PQ66 (2N7002K), PQ67 (2N7002K), PQ68 (2N7002K), PQ69 (2N7002K), PQ70 (2N7002K), PQ71 (2N7002K), PQ72 (2N7002K), PQ73 (2N7002K), PQ74 (2N7002K), PQ75 (2N7002K), PQ76 (2N7002K), PQ77 (2N7002K), PQ78 (2N7002K), PQ79 (2N7002K), PQ80 (2N7002K), PQ81 (2N7002K), PQ82 (2N7002K), PQ83 (2N7002K), PQ84 (2N7002K), PQ85 (2N7002K), PQ86 (2N7002K), PQ87 (2N7002K), PQ88 (2N7002K), PQ89 (2N7002K), PQ90 (2N7002K), PQ91 (2N7002K), PQ92 (2N7002K), PQ93 (2N7002K), PQ94 (2N7002K), PQ95 (2N7002K), PQ96 (2N7002K), PQ97 (2N7002K), PQ98 (2N7002K), PQ99 (2N7002K), PQ100 (2N7002K).

[illegible]

BAT_PRS# = HI	Battery Absent
BAT_PRS# = LOW	Battery Present

# KabyLake ULT Power-Up Sequencing (G3-->S0-->S3-->S4-->S5)

